



Category: SABFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. sabfet\_11110.0

**ALD810026 Balances Four 2.5V Supercaps in Series****Description**

Four 2.5V supercaps in series are balanced using the quad supercapacitor auto balancing (SAB) MOSFET ALD810026. ALD810026 has a threshold voltage,  $V_{t_r}$ , equal to 2.60 volts. When the gate-source voltage,  $V_{GS}$ , is equal to  $V_{t_r}$ , the  $I_{DS}$  ON current for M1/M2/M3/M4 is set at  $1\mu A$ . The  $I_{DS}$  ON current of M1/M2/M3/M4 change exponentially with slight changes in  $V_{GS}$ . Each SAB MOSFET  $M_x$  behaves like a voltage sensitive resistor (See sabfet\_11101.0). At  $V_{GS}$  voltages below or above  $V_{t_r}$ , the SAB MOSFET  $I_{DS}$  ON current changes at a rate of approximately 1 decade for every 0.1V change in  $V_{GS}$ . When  $V_{GS}$  drops low enough, the  $I_{DS}$  ON current becomes essentially zero. In this example, the  $V_{GS}$  voltage of each SAB MOSFET M1/M2/M3/M4 is set at approximately 2.5V, which has a nominal  $I_{DS}$  ON current of  $0.1\mu A$ . If the  $V_{GS}$  voltage for the ALD810026 falls below 2.0V, the  $I_{DS}$  current decreases to pA range, which is near zero compared to  $1\mu A$ .

The voltages across M1/M2/M3/M4 automatically self-adjust to accommodate different leakage currents for C1/C2/C3/C4.  $V_1$ ,  $V_2$  and  $V_3$  settle to approximately  $\frac{3}{4}$  (V+),  $\frac{1}{2}$  (V+) and  $\frac{1}{4}$  (V+) respectively, depending upon relative leakage currents of each supercap. With V+ equal to 10V,  $V_1$  is 7.5V,  $V_2$  is 5.0V, and  $V_3$  is 2.5V. The currents through M1/M2/M3/M4 automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding  $V_{GS}$  voltage of  $M_x$  connected across it, at a higher  $I_{DS}$  ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower  $I_{DS}$  ON currents in the corresponding SAB MOSFET until  $I_{DS}$  ON  $\approx$  0. In equilibrium, the total leakage current across both M1/M2/M3/M4 and C1/C2/C3/C4 network is approximately equal to the highest leakage current of any one of C1/C2/C3/C4.

For full schematic diagram and notes, please register and login at [aldinc.com](http://aldinc.com)