Category: FET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. fet_11132.0

ALD1119 Zener Voltage Clamp Circuit

Description

This voltage clamp circuit produces current versus voltage (I vs. V) that has very sharp turn-on and turn-off characteristics and requires zero power in its off-state. The threshold voltage of the ALD1119xx, $V_{GS(th)}$ is utilized to control the turn-on voltage of this voltage clamp circuit. At V_{GS} voltages below $V_{GS(th)}$, the ALD1119xx MOSFET is turned off and its drain current Ids decreases exponentially with V_{GS} decrease.

At $V_{GS} << V_{GS(th)}$, the gate of the power PMOS is pulled towards V_{DD}, turning the power PMOS off. In this state, the quiescent power dissipation of the circuit consists of essentially leakage currents of the ALD1119xx and the power PMOS. When the V_{GS} ($V_{GS} = V_{DD}$) of the ALD1119xx reaches its $V_{GS(th)}$, it turns on and conducts current to pull its drain voltage toward GND, thereby turning on the power PMOS as well. The current supplied to load R is limited by the $R_{DS(on)}$, current of the power PMOS device which, in this example, is about 0.9A. By selecting different values of R_{BIAS}, the circuit can be turned on at slightly higher (or lower) V_{GS} from $V_{GS(th)}$ of the ALD1119xx. This circuit works from about V_{DD} =2.0V to V_{DD} = 5V. For higher voltages from 5V to 10V, it may be necessary to stack two or more ALD1119xx devices on top of each other.

For full schematic diagram and notes, please register and login at aldinc.com