



Category: FET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. fet_11132.0

ALD1119 Zener Voltage Clamp Circuit

Description

This voltage clamp circuit produces current versus voltage (I vs. V) that has very sharp turn-on and turn-off characteristics and requires zero power in its off-state. The threshold voltage of the ALD1119xx, VGS(th) is utilized to control the turn-on voltage of this voltage clamp circuit. At VGS voltages below VGS(th), the ALD1119xx MOSFET is turned off and its drain current Ids decreases exponentially with VGS decrease.

At VGS << VGS(th), the gate of the power PMOS is pulled towards VDD, turning the power PMOS off. In this state, the quiescent power dissipation of the circuit consists of essentially leakage currents of the ALD1119xx and the power PMOS. When the VGS (VGS = VDD) of the ALD1119xx reaches its VGS(th), it turns on and conducts current to pull its drain voltage toward GND, thereby turning on the power PMOS as well. The current supplied to load R is limited by the RDS(on), current of the power PMOS device which, in this example, is about 0.9A. By selecting different values of RBIAS, the circuit can be turned on at slightly higher (or lower) VGS from VGS(th) of the ALD1119xx. This circuit works from about VDD =2.0V to VDD = 5V. For higher voltages from 5V to 10V, it may be necessary to stack two or more ALD1119xx devices on top of each other.

For full schematic diagram and notes, please register and login at aldinc.com

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