



Category: MOSFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. fet\_11125.0

### ALD1109xx Zener Voltage Clamp Circuit

#### Description

This voltage clamp circuit produces current versus voltage ( $I$  vs.  $V$ ) that has very sharp turn-on and turn-off characteristics and requires zero quiescent power in its OFF-state. The threshold voltage of the ALD1109xx,  $V_{GS(th)}$  is utilized to control the turn on voltage of this voltage clamp circuit. At  $V_{GS}$  voltages below  $V_{GS(th)}$ , the ALD1109xx MOSFET is turned off and its drain current  $I_{ds}$  decreases exponentially with  $V_{GS}$  decrease. At  $V_{GS} \ll V_{GS(th)}$ , the gate of the power PMOS is pulled towards  $V_{DD}$ , turning the power PMOS off as well. In this state, the quiescent power dissipation of the circuit consists of essentially leakage currents of the ALD1109xx and the power PMOS. When the  $V_{GS}$  ( $V_{GS}=V_{DD}$ ) of the ALD1109xx reaches its  $V_{GS(th)}$ , it turns on and conducts current to pull its drain voltage toward GND, thereby turning on the power PMOS as well. The current supplied to  $R_{LOAD}$  is limited by the  $R_{DS(ON)}$  current of the power PMOS device which, in this example, is about 0.9A. By selecting different values of  $R_{BIAS}$ , the circuit can be turned on at a slightly higher (or lower)  $V_{GS}$  from  $V_{GS(th)}$  of the ALD1109xx. This circuit works from about  $V_{DD} = 2V$  to  $V_{DD} = 5V$ . For higher voltages from 5V to 10V, it may be necessary to stack two or more ALD1109xx devices on top of each other.

For full schematic diagram and notes, please register and login at [aldinc.com](http://aldinc.com)