Silicon Gate CMOS Linear Technology

Introduction

Historically, MOS technology has been the domain of the digital designer. Analog designers might use MOS transistors for the input stage of a high input impedance operational amplifier or use discrete MOS transistors in a linear circuit, but bipolar technology ruled the linear integrated circuit world. CMOS technology has changed this. The incredible growth of the CMOS market has caused rapid development of CMOS technology which has led to advanced CMOS linear devices. There are a number of factors that will cause the CMOS linear market to continue to grow rapidly and become a very important part of linear technology. The proliferation of digital circuitry (digital displays, digital computers, etc.) in analog applications, the large increase in chip density, demands for smaller integrated circuits, and the rapid increase in demand for accurate, low power devices will lead to a tremendous number of CMOS linear applications. This article discusses silicon gate CMOS technology and the advantages and disadvantages of the CMOS devices in order for the design engineer to fully understand the role ALD products can play in linear design.

The Technology

Since most linear design is accomplished with bipolar junction transistors, an examination of CMOS and Bipolar Junction Technology (BJT) and the merits of each will best explain the advantages of each technology. Then, a comparison of metal and silicon gate CMOS technology will further identify silicon gate CMOS transistors' unique role.

CMOS technology is "simpler" than BJT technology in that the BJT's three dimensional parameters like base depth, base thickness and base and collector doping do not need to be considered. Since the three-dimensional bipolar parameters are more difficult to control, CMOS technology leads to a better controlled process with less variation in crucial device parameters. In addition, recent advances in processing techniques and equipment are more applicable to CMOS ICs. This means it is likely CMOS technology will advance more quickly than BJT technology. Finally, as the number of chips required per function and the chip count per device goes down, the need for monolithic analog and digital circuitry will increase. CMOS linear devices use the same fabrication process as CMOS digital devices which makes integration of analog and digital devices simple. Bipolar junction transistor technology needs to combine with CMOS technology which makes fabrication cumbersome, complex and expensive.

There is also differentiation within the CMOS world as well as differentiation between CMOS and BJT technology. One major difference is between transistors with a metal gate and transistors with a polysilicon gate. The silicon gate devices derive their advantages from the processing. When making a metal gate CMOS transistor, a mask is used toward the end of processing to allow for proper placement and size of the metal gate. When a polysilicon gate is used, polysilicon is deposited before the gate is defined. The source and drain regions are then doped while keeping the channel doping at a different type. This is known as a self-aligned gate, with which the devices can be made smaller and fabricated with precision. This results in smaller, faster chips with smaller, more stable voltage and current offsets.

Advantages

The major advantages of silicon gate CMOS compared to metal gate linear ICs are their higher speed and lower power consumption. These features impact a broad range of device performance parameters. A faster chip widens the scope of possible applications and increases signal quality and reliability. For a given frequency response, power can be reduced. The CMOS ICs can respond to higher frequency inputs, the timers can oscillate at higher frequencies, and the response times of operational amplifiers and comparators are reduced while slew rate and operating frequency increase. All of these qualities give wider signal frequency range and operating and design margin providing increased accuracy and gain bandwidth at reduced voltages and power requirement over broad operating conditions.

The low power consumptions of CMOS linear chips is advantageous in a number of different ways. Many devices can operate at supply voltages as low as 1V and with ultra low leakage current which facilitates battery operation. This not only means less power consumption, but for operational amplifiers and comparators it results in a lower offset voltage caused by thermal drift and for timers it results in higher accuracy and stability. This lessens the dependence of timing accuracy on expensive components, increasing the accuracy and reducing the cost of the timing function. In addition, as the number of transistors per chip increases, the low power consumption of CMOS ICs allow greater densities but will require little or no external cooling and very little self-heating design considerations.

Another advantage of silicon gate CMOS linear technology to be discussed here is its compatibility with CMOS digital technology. The availability and relative ease with which digital functions such as logic gates, flip-flops, counters and memory cells can be added to the analog library means that complete systems, including a large amount of digital logic, analog modules, and passive components such as resistors and capacitors, can all be integrated into one ASIC chip. This capability is referred to as mixed mode (analog and digital) integration where most components of an electronic system are implemented in a single monolithic IC chip. Generally, in a given system only a few other types of components such as transducers, sensors, inductors, precision resistors, large capacitors, relays, etc. are left off the IC chip.

The final advantage of CMOS linear technology is high circuit function density and low cost. As CMOS linear technology is a VLSI (very large scale integration) technology, many circuit function blocks can be integrated onto the same monolithic IC chip, not only producing compactness, and system miniaturization, but also producing low per function cost and high per function reliability. Furthermore, due to integration of large number of elements, board area cost, labor cost and inventory management costs are greatly reduced.

Disadvantages

In spite of the many technological advantages, there are some disadvantages associated with CMOS linear devices. Although not important for all applications, CMOS devices often lack the current drive capability of BJT's. Noise can also be a drawback of CMOS linear ICs. CMOS has an advantage in its low level of shot noise, but its 1/F noise is larger. The final disadvantage is speed performance and ultra precision for certain applications.