A New Generation of Analog Voltage Comparators

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Introduction

For decades, analog voltage comparators have found a wide range of applications in mixed signal sensor circuits, those used to compare physical measurements that could be translated into corresponding electrical signals. However, historically, voltage comparators are not often used in many precision applications, in part because the input signal source tended to be too weak and consequently inadequate for driving the input of a voltage comparator directly. These precision applications typically required a front-end signal conditioning circuit.

With increased military, homeland security and other industrial applications, for sensitive instrumentation in mobile platforms, there is an increasing need to detect trace molecular amounts of chemical, biological and radioactive elements. As more sensitive, higher precision sensors and detectors are introduced for these tasks, there is also a growing need for higher precision analog voltage comparator with very low-level input signal detection capability. Sensors and detectors that fall into this category include a variety of magnetic, capacitor-based, mechantronics, chemical and radioactive devices that detect traces of particles, elements and molecules. Traditional analog voltage comparators can overwhelm faint signal sources at the input stages with loading effects, even when input signal power requirements are only in the range of 200 to 1000 pW. Frequently these errors seriously limit voltage comparator use where sensors only generate sub-millivolt output signals. For this type of application an improved analog voltage comparator design with maximum input signal sensitivity and correspondingly, minimum introduced error effects is required.

Both the need for direct analog sensor input and the need to have reduced input errors call for a new higher performance voltage comparator. To meet this need ALD is introducing a state-of-the-art Dual Voltage Comparator, the ALD2321, which has the highest rated input signal sensitivity even when compared to the best available in the market. Its input signal power is rated at a maximum of only 0.004 pW _ this represents a 50,000:1 improvement over conventional, industry standard voltage comparators.

Performance Criteria

Leading edge high performance voltage comparators have one of the following attributes: high speed; low input offset voltage; or low input bias current. For the most part, one does not expect to find more than one of the three attributes in the same voltage comparator.

Selecting a high-speed voltage comparator is usually associated with selecting a part with a hefty price tag and a power bill to match, and one also has to live with other compromises such as high input offset voltage and high input bias current. These types usually detect large signals at low resolution and are therefore used for more specialized applications where speed is the only selection criteria.

Select a low input offset, analog voltage comparator, usually built using bipolar technology, and you pay a high premium in almost everything else, especially unit cost and high input bias currents. High input bias currents tend to load down the signal source, introduce errors in the signal source itself, therefore causing erroneous comparator output data. In this example, the output from such a voltage comparator is obviously not the result of an accurate voltage comparison.

Selecting low input bias current as a key specification usually means selecting CMOS voltage comparators. Many CMOS voltage comparators on the market do a good job at relatively low cost from the standpoint of minimizing input signal loading. For many years, ALD's product line included a broad selection of high performance CMOS voltage comparators. CMOS voltage comparators offer very low input bias currents, which in many applications is a paramount consideration. Generally, however, these voltage comparators compromises on having high input offset voltages, which precludes them from many other applications that remain in the domain of bipolar counterparts.

A New Type of Analog Voltage Comparator

Advanced Linear Devices, Inc. has developed, as a result of addressing these above-mentioned considerations, a new type of analog voltage comparator, called the EPAD® analog voltage comparator. This voltage comparator supports the most precise signal detection available on the market, capable of sensing signal levels that were, for the most part, previously undetectable. This new EPAD voltage comparator is the only product on the market that offers both low input offset voltage and low input bias current in a single package.

While implementing a variety of unique “industry first” circuit functions, the major technological breakthrough lies in the use of EPAD® technology for electronically trimming each device for minimum input offset voltage – thereby improving on the earlier comparator to permit the detection and comparison of extremely small input signal differences.

The basic concept behind this new introduction is to first develop a premium grade CMOS voltage comparator, using a low leakage CMOS process. A critical input-offset-voltage adjustment function is then incorporated into the design and testing, so that the input offset voltage can be trimmed to very low offset levels. A simplified diagram of such a voltage comparator is shown in **Figure 1**. An EPAD® MOSFET device is connected to the output of the comparator input stage through an input offset adjustment circuit. This simultaneous achievement of very low input offset voltage **AND** very low input bias current at **ONE AND THE SAME** input terminal is setting a new level of analog voltage comparator performance. Add into this mix higher speed performance, and a new class of high-performance analog voltage comparators is born.

EPAD® voltage comparators improve the combined input offset voltage and input bias current electrical characteristics by up to several thousand percent over the current state-of-the-art voltage comparators available on the market, including CMOS voltage comparators currently offered by ALD. The amount of input power, or energy per second, required to be delivered by a sensor in order to be detected, as measured by the input voltage multiplied by the input current, is reduced by a hundred fold or more. Input signal levels at as low as 0.2 mV and 20 pA can be reliably detected without the need for additional input signal amplification. This translates to about 4 femto-watt (4×10^{-15}), or 0.004 pJ per second. This value is so low that this new voltage comparator allows, for the first time, some sensor and detector systems to be designed with a new design approach, with drastically simplified circuits to amplify and condition the input signal at reduced system cost.

Structural Feature Analysis

The ALD2321 Dual Voltage Comparator is basically a high performance op-amp designed for open-loop operation with multiple output configurations, rapid response times, a small overdrive voltage, ultra low input offset voltage and ultra low input bias currents. Each voltage comparator is factory trimmed for minimum input offset voltage at ground potential using ALD’s exclusive EPAD® Technology.

Each input terminal of this voltage comparator connects to a MOSFET device. The MOSFET is an insulated gate device, which requires only a tiny input current from the input signal and controls the input stage through primarily controlling the input gate voltage. This is in direct contrast to a bipolar input device, which requires a comparatively high input base current to drive the input stage and bias the input bipolar transistor to the proper bias level. The bipolar base input current is generally in the range of 10 nA to 20 nA for a very good, high performance, bipolar voltage comparator. By comparison, many CMOS voltage comparators have input bias currents specified in the range of 100 pA to 200 pA, which is about ten times less than their bipolar counterpart. Through diligent design effort and years of experience, ALD has reduced this input bias current to a guaranteed limit of 20 pA, or about 1% of that of a state-of-the-art expensive, high performance bipolar voltage comparator. This limit is in reality only limited by the practical test and cost considerations. When customized, even lower input bias current and input signal power specifications can be specified and tested for this voltage comparator.

A classical CMOS voltage comparator requires a signal voltage of several millivolts, and typically requires an additional overdrive voltage of up to 100 mV in order to drive the internal circuits. The new analog voltage comparator, by contrast, requires only a fraction of that voltage from the signal source in order for it to operate properly. This is accomplished with an enhanced internal gain stage while providing level shift buried deep inside the voltage comparator. The gain stage increases the input sensitivity and at the same time enables a more muscular output driver.

Traditional CMOS voltage comparators suffer from inadequate output drive and thus often require another external buffer stage, even if the output drive requirements are relatively modest. The most common of external buffers used in this case is a bipolar NPN transistor or a Power MOSFET driver. While not expensive and abundantly available, they do add extra components on the printed circuit board. The new EPAD® voltage comparator includes an enhanced on-chip output driver stage that increases the output drive current by about tenfold, compared to a typical CMOS voltage comparator available on the market. This is actually accomplished at a rather modest increase in chip cost. This output driver eliminates the need for an external driver in many types of applications, achieving overall board cost efficiency by reducing or eliminating extra components. The end result is an instrument grade, high-integration-level high-precision voltage comparator sub-system implemented on a single IC chip that optimizes the entire voltage comparator function from input front-end stage to the output back-end stage.

One other noteworthy feature is the dual digital complementary outputs for each comparator that allow configuration of up to two outputs for each voltage comparator. Each output can be independently wired as a single-ended, multiple wired-or, or push-pull complementary driver. In the open-drain configuration, the output voltages can exceed the positive supply voltage. In a dual package, one voltage comparator output can be configured as push-pull output while the other is set up as open-drain output, giving the designer a broad range of functional options using this all inclusive single-chip solution.

How EPAD® Technology enhances Voltage Comparators

The EPAD® voltage comparator is carefully designed through the wafer fabrication process for optimized matching of the two input stages, one for the sensor input signal and the other for the reference input. However, the accumulation of photolithography and thermal cycle mismatches as well as small masking variations may result in an accumulated input voltage imbalance between the two input stages. Ironically, semiconductor fabrication and assembly processes themselves are rather hostile to avoiding “extraneous environmental conditions”. Meanwhile, an EPAD® (Electrically Programmable Analog Device) MOSFET device is embedded and attached to the output of each of the two input stages. At each manufacturing step, minute errors accrue to the input of the voltage comparator, as would be the case in the semiconductor manufacturing of any IC component. Some additional errors also accumulate at this MOSFET device.

At the near completion of the manufacturing cycle, this MOSFET device is called upon to perform a computer-automated calibration, or “e-trim”. At that point, any accrued residue device matching errors between the two input stages are measured and corrected. Note that this error correction is performed at the near completion of manufacturing, where the potential to maximize error elimination is the greatest. This sequencing of the manufacturing steps is important because many manufacturing process steps in the semiconductor process requires high temperature or high mechanical stress, which in turn tend to alter slightly the characteristics of the sensitive circuit it is producing.

Finally, the device is carefully and thoroughly tested on an automated test system. The primary objective is to insure the device(s) experience a minimal level of extraneous environmental stress conditions outside of normal conditions after “e-trim”. Upon a final quality inspection, the device is ready for delivery.

EPAD® Technology and E-TRIM™ Trimming

EPAD® is an acronym for Electrically Programmable Analog Device – a patented and trademarked technology developed by ALD to precisely electrically trim, or e-trim, CMOS analog integrated circuit elements at the package level. EPAD® is a proven design and manufacturing technology first conceived by ALD almost twenty years ago. This technology has been steadily improved over the years and has been applied to increasing array of analog components produced by the company.

When included in a circuit design, the EPAD® function is analogous to having multiple on-chip “trimmer potentiometers”, each set to a different desired voltage level. The EPAD® function consumes a very small die area, and can be e-trimmed as part of the fully automated circuit testing. Hence, EPAD® is a cost effective way to enhance performance. EPAD® circuit elements can be integrated in operational amplifiers and other popular linear circuits, as well as voltage comparators. For example, ALD offers dual and quad EPAD® devices as separate packaged products, the ALD 1108E and ALD 1110E, as well as a family of single and dual EPAD® Operational Amplifiers, i.e, the ALD1721 and ALD2721.

These products can be e-trimmed by the end user, including in-system e-trimming, using software and hardware available from ALD. Once trimmed, the device voltage and current characteristics are stored indefinitely in the chip even when the power to the chip is removed. MOSFET devices are part of a circuit element that can be electrically trimmed in up to thousands of small, incremental steps. Programming or trimming is achieved through a series of short, software controlled voltage bursts to a floating gate MOSFET structure. The floating gate is a layer of polysilicon embedded within the gate oxide**.** A cross section diagram of the floating gate structure is shown in **Figure 2.**

When integrated into a CMOS voltage comparator, the EPAD® MOSFET resides right after its input stage, and sits embedded inside the chip to wait until substantially all the other manufacturing stages of the voltage comparator are completed. At that point, an additional manufacturing step is added, which provides automated programming of this embedded EPAD® MOSFET and its associated circuitry. Generally this is also referred to as the " e-trim" step of the manufacturing process. In **Figure 3**, an automated EPAD®-based station consist of a PC controller, a hardware module that provides the measurement, switching logic and the e-trim voltage pulses to inject charge under software control, and a device specific adapter.

The e-trim operation is basically a factory-performed function, which is mostly invisible to users of these devices. For certain users, who may have a requirement to manually trim after installation, or who may desire to conduct their own automated in-system trimming, programming modules are available for basic e-trim applications. For more extensive production-line trimming and automated in-circuit trimming applications, various custom application packages are available from ALD.

Application Example

One of the most significant features of the new analog voltage comparator is the small input signal power specification, which makes it ideal for applications that require either exceptional precision or where the signal to be detected is very weak. Very small signal are output from many types of sensors and detectors based on integration of electron charge that is the direct result of particles, photons or elements being in the path of a physical parameter to be detected. These types of devices and associated applications are prime candidates to benefit from this new analog voltage comparator.

An example of such an application describes how the level of sensitivity and accuracy of a detector system can be greatly improved using this new voltage comparator. The application is to detect the output signal of a device at a very small output current. This output signal is controlled by an input voltage ramp that provides a trickle charge current to an integrating capacitor. (See **Fig. 4.** EPAD® Voltage Comparator Application Example: Sample and Hold Circuit with Ramp Generator).

The charging rate of the integrating capacitor is 100 millisecond per volt. The object is to detect the output voltage of an Output Device within 2 mV resolution at a specified output current level that ranges from 1nA to 1uA. The output voltage and current of the Output Device has a non-linear dependence relationship with the voltage on the integrating capacitor. Once a desired voltage level is reached at the integrating capacitor, the voltage comparator needs to quickly stop the charging current so that the input voltage level can be accurately measured.

In summary, this circuit is a kind of a sample-and-hold circuit with a precise trigger threshold. It is implemented by using a low-charge-injection analog switch, such as the ALD4213, which transitions in about 100 nanoseconds. In order to keep the output voltage level as accurate as possible, it is necessary to not have any significant leakage current across the integrating capacitor and at the Output Device. Of course, the Output Device does need to be connected to the voltage comparator in order for its output voltage to be measured. Hence the input bias current level of the voltage comparator directly controls the accuracy of the voltage detected across the Output Device.

This input bias current also directly limits the output current range of the Output Device. A bipolar voltage comparator with high input bias current would limit the current range too severely to be useful. Based on a 20 nA input current in a typical bipolar device, and assuming 1 % accuracy desired, the lowest current the output device can handle is 2 uA, which is completely out of the range of measurement. At the low end of the detection range, the output current is only 1 nA whereas the bipolar voltage comparator draws up to 20 nA! Hence this type of circuit cannot be implemented by using a bipolar voltage comparator.
A traditional CMOS voltage comparator with low input bias current specification can handle the leakage current requirements, but the error of detection would be hundreds of times greater, because the voltage comparator input offset voltage would

directly limit the trip voltage of the circuit. A CMOS voltage comparator with +/-10 mV input offset voltage would produce up to 20 mV of measurement window.

The time it takes for the voltage comparator to produce a valid output signal also limits the accuracy of the entire system. As the integrating capacitor is still charging, any delay time from the voltage comparator trigger threshold voltage to the switching off of the input ramp voltage adds directly to an error voltage. Any additional time taken to stop the ramp voltage must be part of the overall error budget. Using the ramp voltage of 100 millisecond/V, a 25 microsecond delay would add 0.25 millivolt detection error. However, the actual detection error is much greater, because of the comparator overdrive voltage requirements. If a voltage comparator requires an overdrive of 100 mV, then the error is 100 mV + 20 mV, or about 60 times greater than the entire error budget!

Using the new analog voltage comparator ALD2321, instead of bipolar or traditional CMOS voltage comparators, the error budget adds up to an estimated 1.45mV, which is within the error budget (input offset voltage + delay in overdrive + the ramp voltage switching error = 0.4 mV+1 mV +0.05mV). . This is an example of a type of detection circuit that has not been possible to make using conventional analog voltage comparators prior to the arrival of the new ALD2321!

An optional method of achieving this level of detection is to use a computerized test system costing well over $30,000 and at the expense of taking a long time, up to several minutes, for computation and measurements on such a system to iteratively measure and compute each data result. With the new analog voltage comparator ALD2321, the job is done with just a few IC components at low cost, and the result is dramatic. Not only is the measurement result using the new voltage comparator circuit more accurate than that of the test system, the result is obtained in less than 1 second!

Conclusion

In many transducer applications it is necessary to convert very low level analog signals into digital information for faster and more accurate signal processing. Examples of such transducers include photodiodes, shaft-position pickoffs, capacitor-based sensors, radioactive cavity sensors, magnetometers and other zero crossing sensors – each outputting very low signals e.g., sub-nanoampere and at sub-millivolt. Using a voltage comparator, acting as a simple A/D converter, is a preferred technique for digitizing these signals. A new class of signal detection circuit and higher level of accuracy and sensing is needed to address these low levels of signal detection challenges we now face. A new class of voltage comparator, an EPAD ® voltage comparator, can perform many of the circuit functions required to translate these low signal levels into usable digital data. With the introduction of the EPAD® voltage comparator, that frontier of tiny signal detection has just been advanced to a new horizon.

Although the venerable voltage comparator is not a new invention, ALD has taken a fresh look at the market and the basic function it performs and has taken a creative approach to address present day challenges to this widely used component. The key to this high-performance analog voltage comparator is twofold. First, a novel technique based on a proprietary proven technology breathed new life into a component that is still evolving and growing in use, due primarily to the new classes of sensors and the new demands on better detection they place on the voltage comparator. Second, ALD has taken advantage of higher levels of integration with a modern semiconductor process to incorporate more functions into a single IC chip. These functions include an enhanced input amplifier stage, intermediate gain stage, and an output buffer amplifier, which in combination enable the entire job from low level input signal detection to high output driver all to be performed in a single monolithic sub-system IC chip!

Fig.1 A Simplified EPAD^R Voltage Comparator

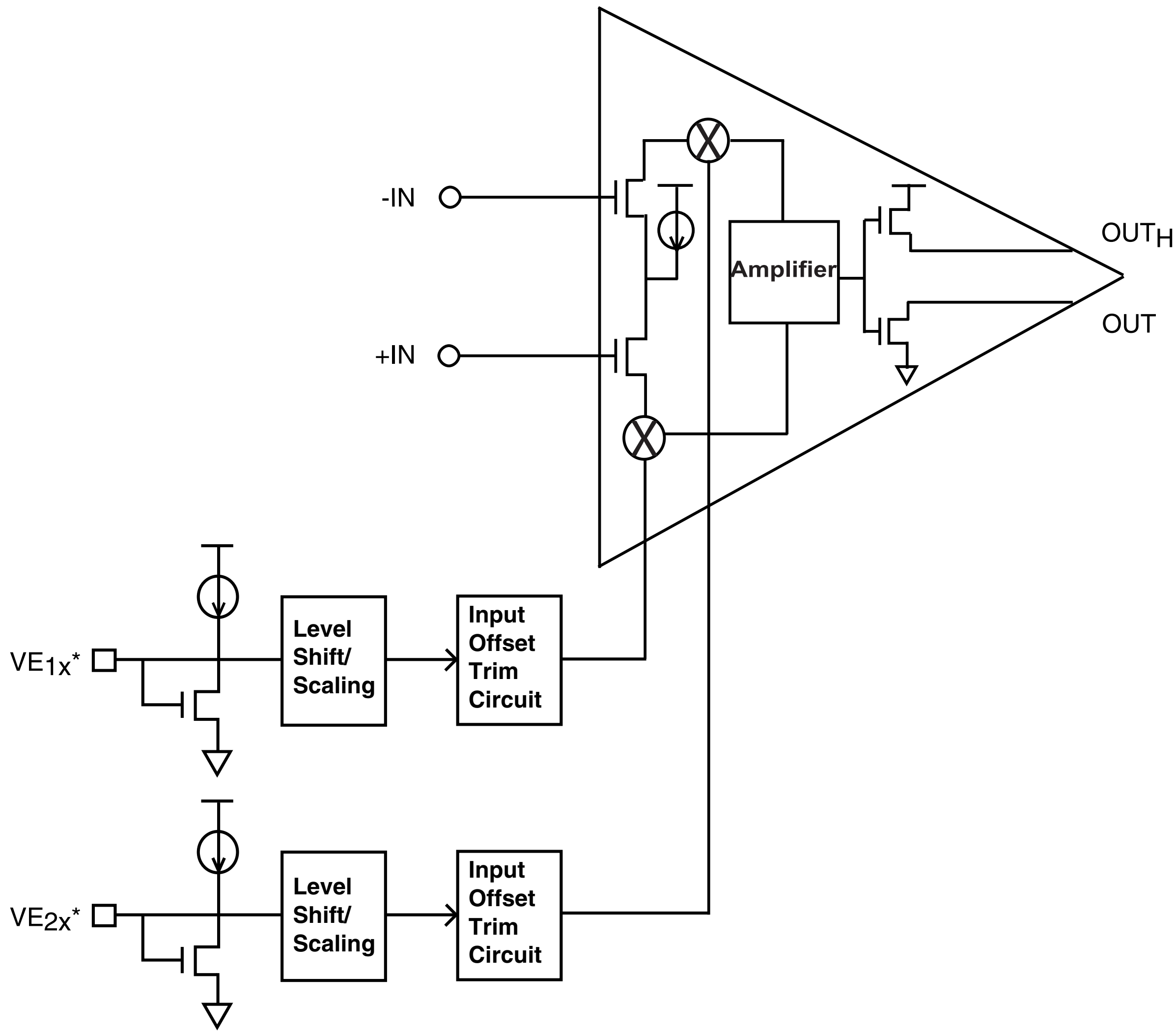
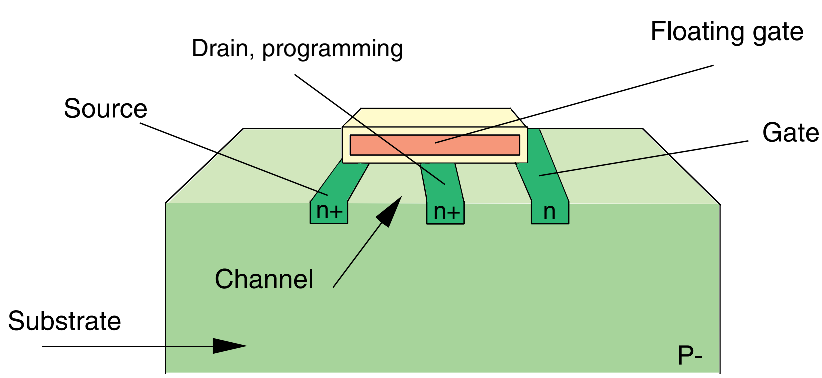


Fig. 2 An Electrically Programmable Analog Device (EPAD^R) Structure



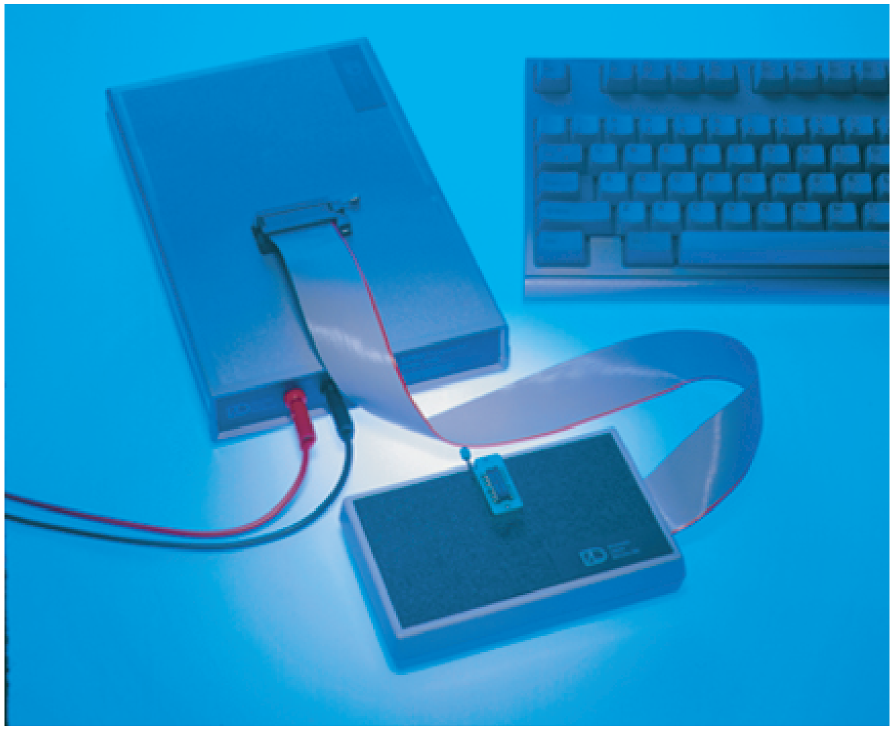


Fig. 3 Automated E-TRIM^{TM} System (Computer not shown)

Fig. 4 EPAD^{R} Voltage Comparator Application Example: Sample and Hold Circuit with Ramp Generator