USING LOW VOLTAGE FET INPUT OPERATIONAL AMPLIFIERS

GENERAL DESCRIPTION

Low operating voltage linear systems, especially battery operated systems such as portable instruments or terminals, tend to have a different set of requirements and constraints placed on them. Usually, for such systems, not only must the linear circuits operate at low voltages, but these voltages tend to vary due to limited power supply regulation or gradual discharge of a battery pack over time. Furthermore, power drain of the system is nearly always a major consideration. In order to lower the operating power dissipation of a circuit, linear active components such as operational amplifiers not only need to have very low operating currents, but the selection of passive components such as gain setting resistors or network feedback resistors must be at as high values as possible, and still meet the precision and frequency requirements of the system.

As an example, a simple DC inverting amplifier connected as a 10X gain amplifier can use a 1kΩ and 10kΩ resistor gain setting network. The maximum current drain through the resistors in a ±15V system may be 1.5mA (24.75mW) and in a 5V system may still be as high as 250μA. Using a low voltage FET input operational amplifier, on the other hand, the resistors used may be a 1MegΩ and 10MegΩ resistor network without sacrificing the gain precision. However, this requires very high input impedances at the op amp inputs such that leakage currents at the inputs would not introduce large errors to the output voltage of the FET op amp set by the 10MegΩ resistor. The current drain due to the resistor network in such a 5V system is drastically reduced to 0.25μA (0.63μW). An added benefit here is that with very low current flow in the resistors, gain errors caused by resistor self-heating effects at different output voltages are minimized or eliminated.

FET operational amplifiers with high input impedance not only help increase the value of an external resistor network, but also operate as near ideal voltage buffers. This is useful for a variety of high impedance sensors and transducers which are essentially charge accumulating devices that supply a voltage output but cannot sustain current flow. Often such devices also produce more current noise effects than voltage noise effects. In a FET operational amplifier, where usually the current noise characteristics are far superior to its voltage noise performance, the overall system noise may be reduced while the voltage noise spec alone might have indicated otherwise.

IMPROVED OPERATING (VOLTAGE) MARGINS

One important factor affecting low voltage applications in general is the actual input and output operating voltage ranges available from the operational amplifier. For example, an input voltage range of ±11V for a ±15V system may be perfectly acceptable for a given application, even though the operational amplifier may need a 4V "overhead margin" from each supply rail. However, for a single 5V system, such an overhead voltage is obviously not acceptable as there would not be any operating voltage left to supply an output.

For a 5V single supply system or a ±2.5V system, a 1V overhead from each supply rail of an operational amplifier would mean only 3V linear operating voltage range, which is not much room to play with. The same circuit when operating at 3V and 2V would have 1V and 0V of actual useful design operating range respectively. From this it becomes apparent that for low operating voltages, rail-to-rail operating voltages may be an imperative rather than a luxury.

In order to implement rai-to-rail voltages (or as wide operating voltage ranges as possible), FET operational amplifiers with CMOS input stages have an advantage. The rail-to-rail operating ranges are usually achieved by using complementary drive design techniques, best implemented by having complementary N channel and P channel input stages. Rail-to-rail outputs can be implemented by class AB output stages using N channel and P channel MOSFETS for push-pull outputs that span the full supply voltage range. MOSFET transistor characteristics tend to assist in accomplishing rail-to-rail outputs because at small drain voltages, both N channel and P channel MOSFET have essentially resistive characteristics. With high impedance loads, such as CMOS data converters, CMOS comparators or CMOS logic gates, the output voltages approach within a few hundred microvolts (less than a mV) of the supply rail voltages. For ratiometric designs that use the power supply rails, rail-to-rail operational amplifiers can provide precision all the way to the rail voltages without introducing significant error.

Another design consideration when using low voltage precision operational amplifiers comes from analyzing some of the specifications themselves. The PSRR and the CMRR (the power supply rejection ratio and the common mode rejection ratio) of a given operational amplifier are

usually specified in dB. However, the effect of these parameters when applied to a low signal voltage application is of interest. Use of large supply voltages, with a large common mode voltage supply, will introduce a larger error signal voltage into an already small signal to be amplified.

As an illustration of this point, first let us take the case of PSRR. A circuit operating at ±15V and using an operational amplifier with PSRR of 80dB would have introduced an error voltage of 100μV for each 1V change of the supply voltage. A 10% ±15 V power supply would have total supply voltage variation of 3V. The equivalent input offset error voltage introduced by PSRR would therefore be 300 μV. Now consider an operational amplifier having the same PSRR spec but operating at 2V. A 10% variation of a 2V supply now introduces 0.2V change to the supply voltage for the part. The operational amplifier with the same 80dB PSRR spec would now only introduce a 20μV error.

REDUCED POWER SUPPLY AND COMMON MODE ERRORS

Now consider CMRR which is also usually specified in dB. An operational amplifier with 80 dB CMRR at ±15V with a voltage signal equal to 50% of the supply range would see ±7.5V voltage excursion and a 1.5mV equivalent offset voltage error introduced into the signal. In comparison, the error voltage for a low voltage operational amplifier at 2V supply, with 80 dB CMRR and 50% signal range would be 100 μV instead. In this case the percentage error introduced into the signal may be the same, but a 1V peak signal compared to a ±7.5V peak signal, both having 50% signal voltage range, would in actual fact have quite different absolute error voltages introduced.

OUTPUT CURRENT DRIVE

Another anomaly to consider in adjusting the intuitive process to low voltage circuit design, especially for an experienced analog designer accustomed to using ±15V operational amplifiers, is the output current drive spec. For a 2kΩ load in a ±15V (30V) system, to drive the output to a voltage close to full scale would require 7.5mA output drive current. The same 2kΩ load in a ±2.5V system would only require 1.25mA from the output stage. Of course high power output drive is not quite compatible with low voltage operational amplifier applications, but the point is that one can be fooled with the intuition that low voltage operational amplifier applications require the same high output currents as their higher voltage cousins when driving a similar impedance load.

Using FET operational amplifiers, circuit designs are often simplified due to design considerations such as input bias and offset current effects, where these effects are considered to have negligible effect upon the performance of the design task at hand. Variation of a very high input impedance would not impact a design if the worst case minimum input impedance under all circumstances is acceptable. This reduces the need for current compensation with bias balance resistors and noise bypass resistors. The high impedances inside a circuit network also tend to reduce current spikes in the power supply line, minimizing any signal and load induced variation of the power supply. This is especially true for high impedance power supply sources such as batteries. Lowered current spikes in a circuit reduce the need for local supply bypass capacitors, and frequently, even when a bypass capacitor is deemed necessary, a single one can be used to serve many operational amplifier circuits.

IDEAL FOR HIGH PERFORMANCE SIGNALS

Low voltage FET operational amplifier circuits excel when high source impedance device applications are considered. These applications include a class of devices such as high impedance bridge networks, capacitive sensors, pH probes, humidity sensors, diode detector arrays and pressure sensors. A single supply FET operational amplifier is often a suitable choice for interface circuits that perform the tasks of buffering, amplification, signal conditioning and linearization, and temperature compensation. A low voltage power source may, in this case, bring significant additional cost savings to the system due to reduced power rating requirements for the system. High in-circuit element impedances can also mean easier single supply to dual supply circuit conversion. For example, in single supply linear systems there is often a need to generate a virtual ground which acts as a reference point for some of the positive and negative transition analog signals. This reference can be generated simply and very inexpensively by using two large resistors in a voltage divider with a bypass capacitor, providing that only a voltage with no current supplying capability is required. In a FET operational amplifier circuit, conditions are frequently right for just such a reference.

High in-circuit impedances do make the system more vulnerable to noises, both generated internally within the system components and coupled from outside. Internal to the system higher impedance means less di/dt caused coupling noise. However, higher internal circuit impedances may require careful grounding of the circuit board and perhaps some degree of shielding. The amount of grounding and shielding is a function of a given application and its level of susceptibility to the environment in which it is expected to operate.

HIGH RELIABILITY

Often, low voltage FET operational amplifier designs not only imply low power operation but also provide improved reliability. For example, a circuit with 5 V and 1 mA power drain uses 5 mW whereas a circuit with 30 V (+/- 15 V) and 1 mA burns 30 mW of power. The difference in power dissipation means less self-heating for a low voltage circuit and therefore lowered operating chip junction temperature.

The unit, when first powered up, reaches stable operating temperature virtually instantly and introduces less self-heating induced errors into the signal. Cooler operating temperature also implies better reliability and longer term drift as almost all components operate more reliably at reduced temperature. These factors can make a low voltage FET operational amplifier implementation of a circuit an attractive choice even if lowered power drain is not a primary objective.

APPLICATIONS

As previously mentioned, the primary advantages of using low voltage FET operational amplifiers are high input impedances, low power dissipation and relative ease of using large resistors and small capacitors in the circuit networks. As a result, many applications can be simplified. Figure 1 illustrates some of these advantages in a single supply amplifier circuit with a self generated signal reference. The signal reference is accomplished simply by adding a resistor R3 to the normal gain feedback resistor network consisting of R1 and R2. The input is amplified in the non-inverting mode and provides high gain referenced to the DC voltage set by the resistor R3. Vin range of 0 to 20 mV would be amplified with a gain of 100X and give outputs from 0V to 2V.

Other typical FET operational amplifier applications include micropower inverting amplifiers, two stage single supply non-inverting amplifiers and charge integrators as shown in Figure 2 to Figure 4b. These circuits can provide precision set by the external components with very low error introduced by the input bias currents and input offset currents. Two circuits that take full advantage of low input bias currents of FET operational amplifiers are the non-inverting amplifier, Figure 5, and the unity gain non-inverting amplifier, Figure 6. In both cases, the input impedance is greater than 1.0 x E+13 Ω.

Classic applications that require FET operational amplifiers are those that depend on low input bias currents, such as current measurement circuits as well as charge measurement circuits. Current to voltage converter, as shown in Figure 7, and current to voltage inverter with amplified gain (Figure 8) are circuits that deal directly with very low level currents as signals. The outputs are low impedance voltage outputs with precision directly proportional to the precision of the resistors R1, R2 and R3. Circuits that depend on charge preservation, such as the Capacitance Multiplier circuit in Figure 9 and the Precision Sample and Hold circuit in Figure 10, have operating frequency range, capacitance range and hold time specifications that depend directly on the input bias current specification.

Another example of a low voltage FET operational amplifier application is a micropower buffered rail-to-rail adjustable voltage source. In the circuit the voltage setting potentiometer can have a large value using very little direct current drain across the power supply rails. This voltage is then buffered with a FET input CMOS operational amplifier such as an ALD1701 that swings from rail-to-rail, as shown in Fig. 11. Although the circuit appears straightforward and simple enough, actual implementation of this function would have been complex and relatively difficult without a rail-to-rail FET input operational amplifier that handles both high input impedance and complementary FET input voltage range requirements simultaneously.

A more esoteric group of circuit function is the logarithmic and anti-logarithmic circuits, Figure 15 to Figure 16 By using these circuits, first by converting two input voltages into log values, then a summing function in which an addition of the two converted voltages are performed, followed by an antilog conversion of the result of the summation, one effectively creates a divide circuit function. Figure 17 shows a circuit function that divides input A by input B and provides an output that is the result of the division.

CONCLUSION

In summary, low voltage FET input operational amplifiers face a different set of requirements and challenges, but also provide a unique set of characteristics to meet those challenges. The analog designer may have to look at some of the requirements in a different way and may also need to interpret things differently. In a world where everything is increasingly mobile, portable and transportable, low power drain, low voltage circuits certainly play an increasing role. Low voltage FET input circuits, such as CMOS operational amplifiers, are becoming increasingly important participant in this trend.

APPLICATIONS

Figure 1 Single Supply Amplifier with Self-Generated Signal Reference

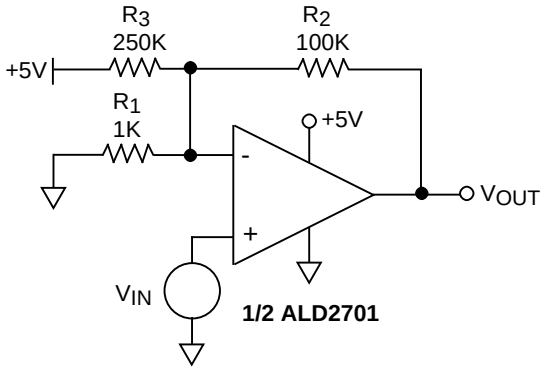
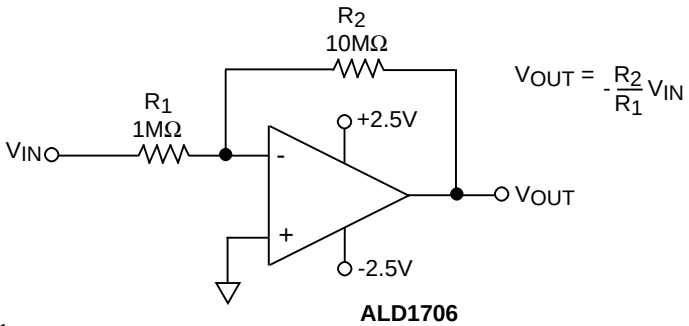


Figure 2 Micropower Inverting Amplifier



Note: Gain of 10 amplifier
Input impedance is limited to R_1.
Total typical current drain of 20µA

Figure 3 Two Stage Single Supply Non-Inverting Amplifier

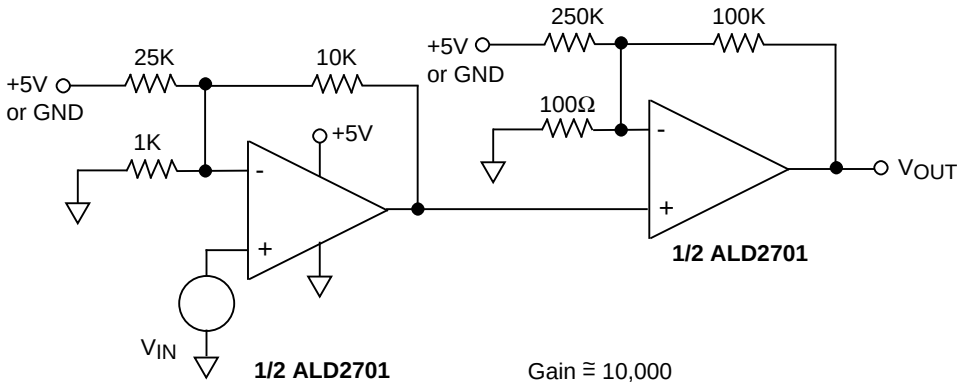
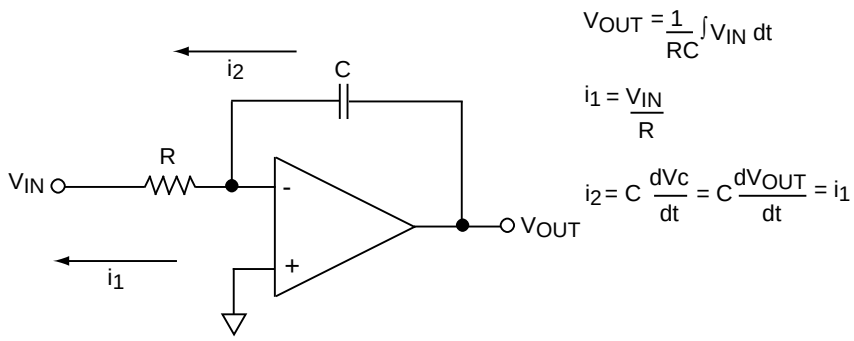


Figure 4a Integrator



Note: This circuit forces a current i_1 on the summing junction and causes the output to ramp at a rate of $\Delta Vout/\Delta t$ equal to i_1. It is set by input resistor R and input voltage Vin. It can be seen that any leakage current on the summing junction directly subtracts from i_1 and affect the ramp rate. For long integration time, dt is large and imply small i_2 or large C since voltage swing $\Delta Vout$ is usually limited. For precision applications, amplifier input leakage directly affects the value of i_2 and may be a significant contributor to overall error of integrator.

Figure 4b Charge Amplifier

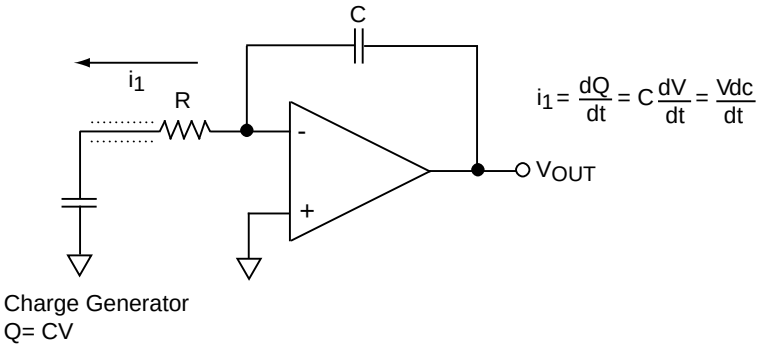


Figure 5 Micropower Non-Inverting Amplifier

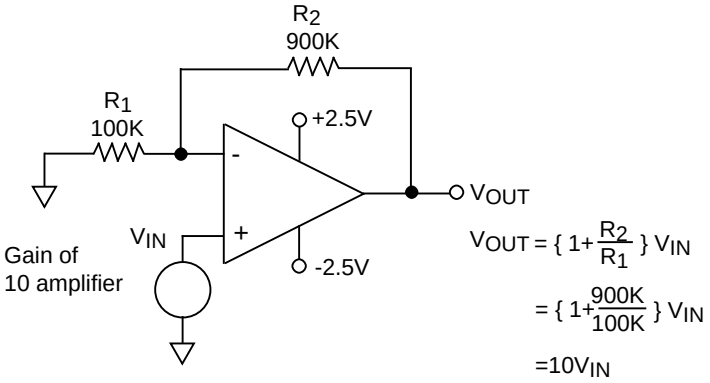
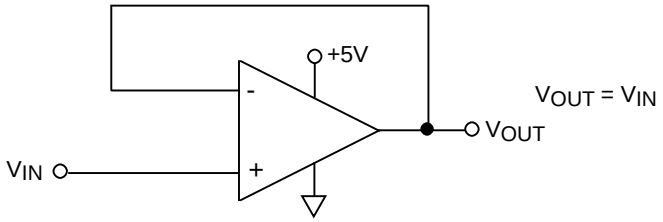


Figure 6 Unity Gain Non-Inverting Buffer



This is extremely effective in providing isolation between input and output. Essentially the source impedance can be open circuit (i.e. capacitive source) while providing drive to resistive load as low as 1kΩ amd capacitive load of 400pF.

Figure 7 Simple I-V Converter

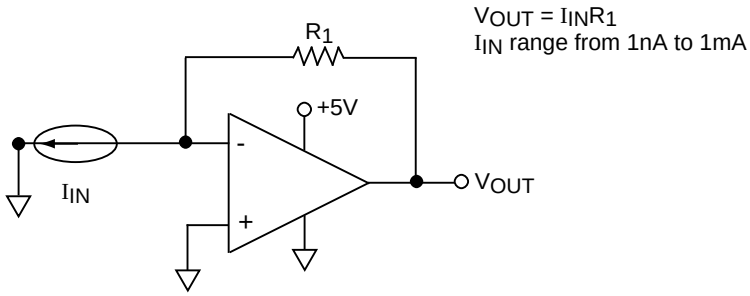


Figure 8 High Gain I-V Converter

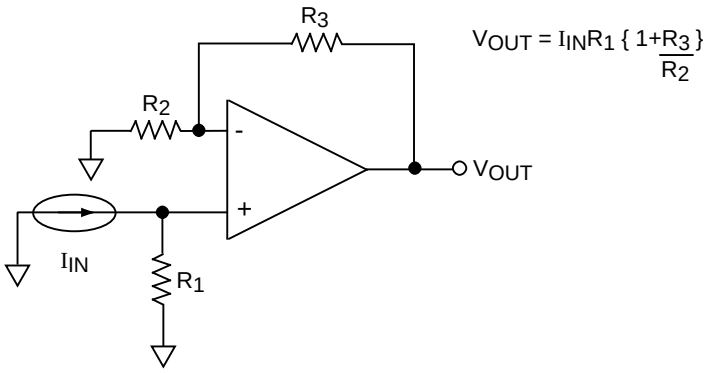
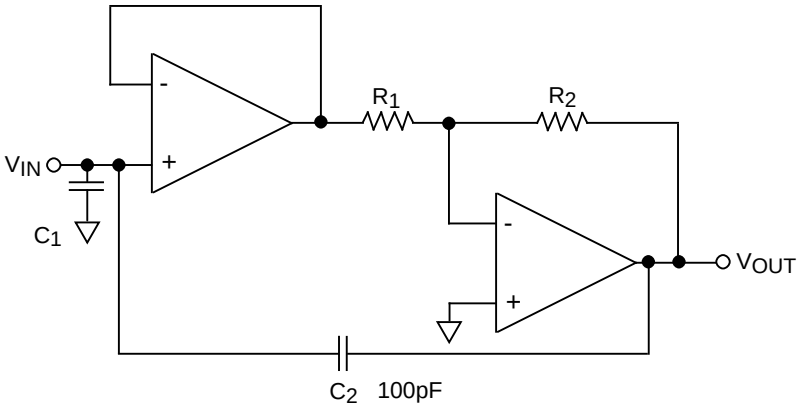


Figure 9 Capacitance Multiplier



$\frac{R_2}{R_1} = 99$ $C_1 = C_2 \{ 1 + \frac{R_2}{R_1} \} = 100 \times C_2$

Figure 10 Precision Sample/Hold

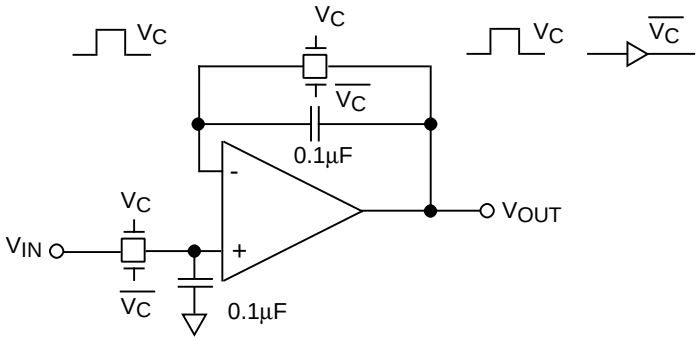
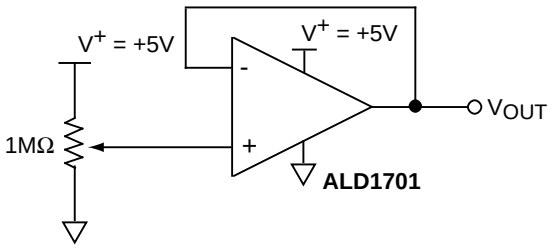


Figure 11 Micropower Buffered Rail to Rail Adjustable Voltage Source



V_{IN} can be set to within 1mV of either power supply rail. The total power dissipation of the circuit is essentially that of the operational amplifier power dissipation of approximately 0.5mW.

Figure 12 Voltage to Current Converter, Inverting Type

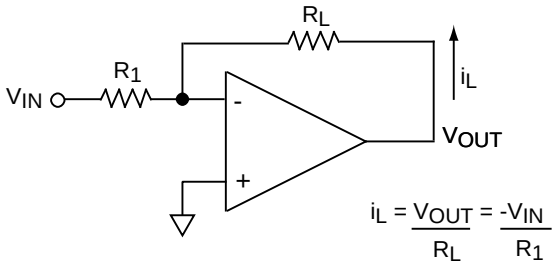
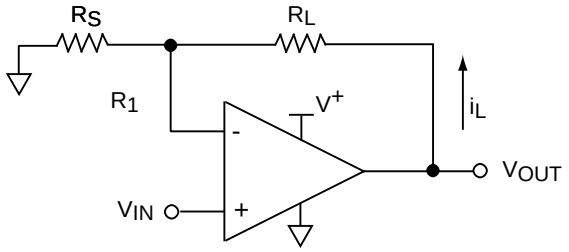


Figure 13 Voltage to Current Converter, Non-Inverting Type



$V_O < V_{IN} < V^+$
V_{IN} Rail-to-Rail, Hi Ƶ Input

$i_L = \frac{V_{IN}}{R_S}$ i_L Independent of R_L

Figure 14 Voltage to Current Converter

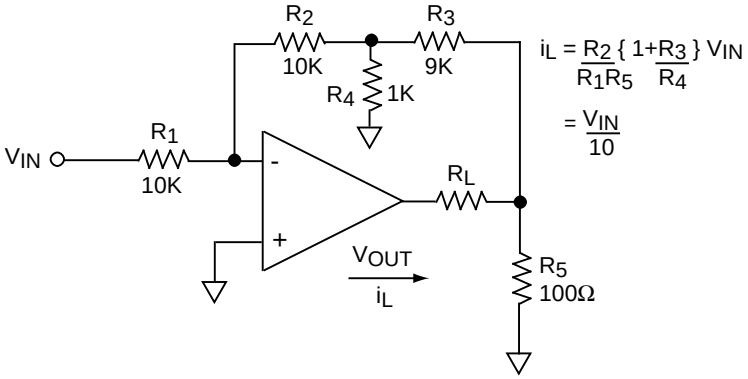


Figure 15 Logarithmic Amplifier

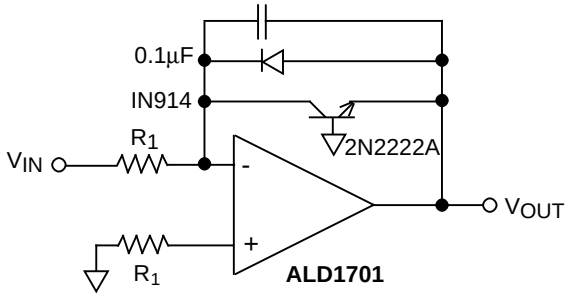


Figure 16 Antilogarithmic Amplifier

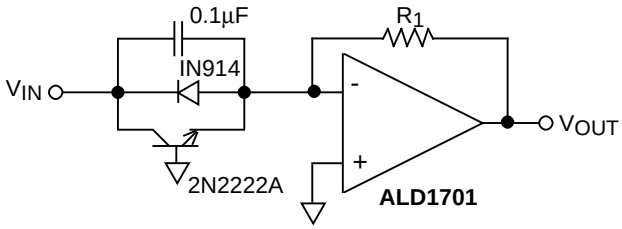
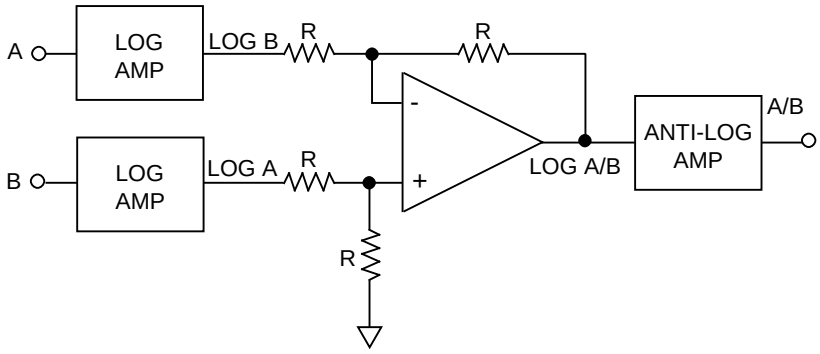


Figure 17 Division of Two Input Signals



For Log Amp circuit, see Fig. 15.
For Antilog Amp circuit, see Fig. 16