



DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is $= 5\text{mA}/50\text{pA} = 100,000,000$.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low V_{os} -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package
- RoHS compliant

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

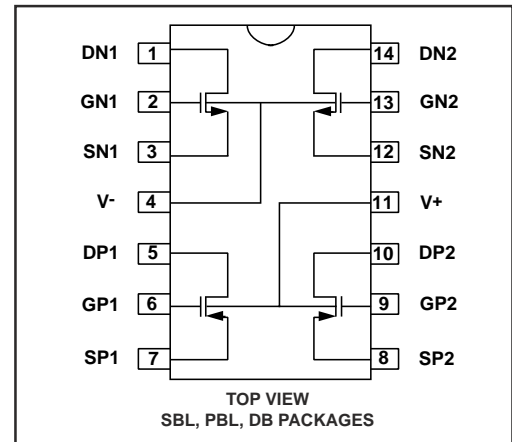
Operating Temperature Range*		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD1103SBL	ALD1103PBL	ALD1103DB

* Contact factory for leaded (non-RoHS) or high temperature versions.

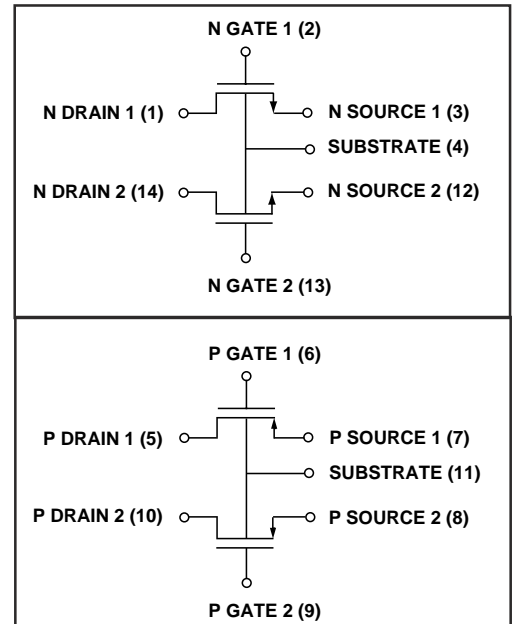
APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V_{DS} _____ 10.6V
 Gate-source voltage, V_{GS} _____ 10.6V
 Power dissipation _____ 500mW
 Operating temperature range SBL, PBL packages _____ 0°C to +70°C
 DB package _____ -55°C to +125°C
 Storage temperature range _____ -65°C to +150°C
 Lead temperature, 10 seconds _____ +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

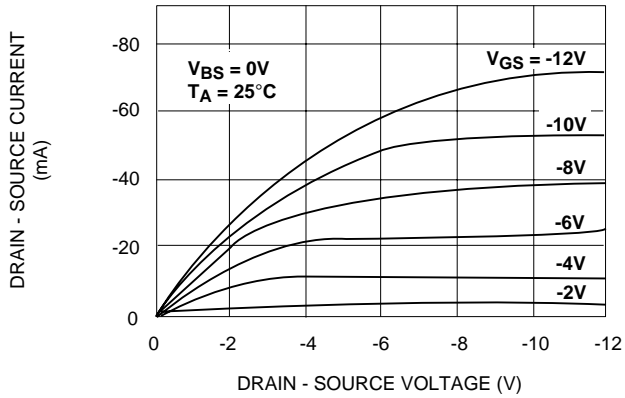
OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ unless otherwise specified

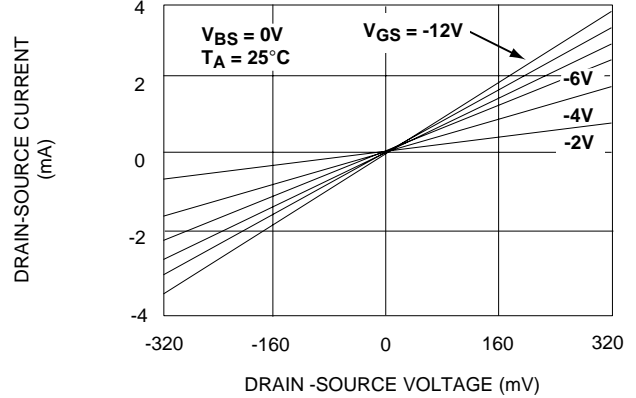
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	V_T	0.4	0.7	1.0	V	$I_{DS} = 10\mu\text{A}$ $V_{GS} = V_{DS}$	-0.4	-0.7	-1.2	V	$I_{DS} = -10\mu\text{A}$ $V_{GS} = V_{DS}$
Offset Voltage $V_{GS1} - V_{GS2}$	V_{OS}			10	mV	$I_{DS} = 100\mu\text{A}$ $V_{GS} = V_{DS}$			10	mV	$I_{DS} = -100\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift	TC_{VT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	25	40		mA	$V_{GS} = V_{DS} = 5\text{V}$	-8	-16		mA	$V_{GS} = V_{DS} = -5\text{V}$
Trans-conductance	G_{fs}	5	10		mmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$	2	4		mmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Mismatch	ΔG_{fs}		0.5		%			0.5		%	
Output Conductance	G_{OS}		200		μmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$		500		μmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Drain Source ON Resistance	$R_{DS(ON)}$		50	75	Ω	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		180	270	Ω	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		0.5		%	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source Breakdown Voltage	BV_{DSS}	12			V	$I_{DS} = 10\mu\text{A}$ $V_{GS} = 0\text{V}$	-12			V	$I_{DS} = -10\mu\text{A}$ $V_{GS} = 0\text{V}$
Off Drain Current	$I_{DS(OFF)}$		0.1	4	nA μA	$V_{DS} = 12\text{V}$ $I_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$		0.1	4	nA μA	$V_{DS} = -12\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	I_{GSS}		1	50	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = 12\text{V}$ $T_A = 125^\circ\text{C}$		1	50	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = -12\text{V}$ $T_A = 125^\circ\text{C}$
Input Capacitance	C_{ISS}		6	10	pF			6	10	pF	

TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

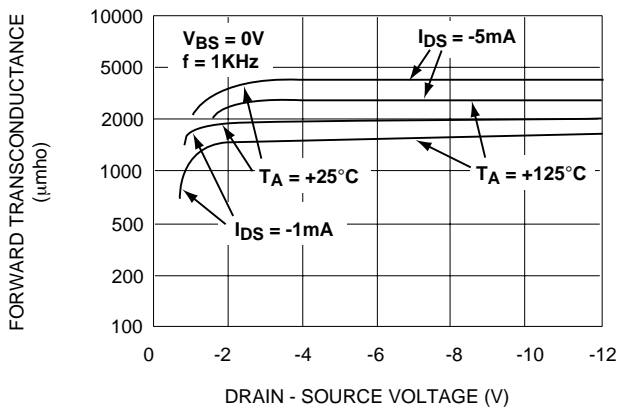
OUTPUT CHARACTERISTICS



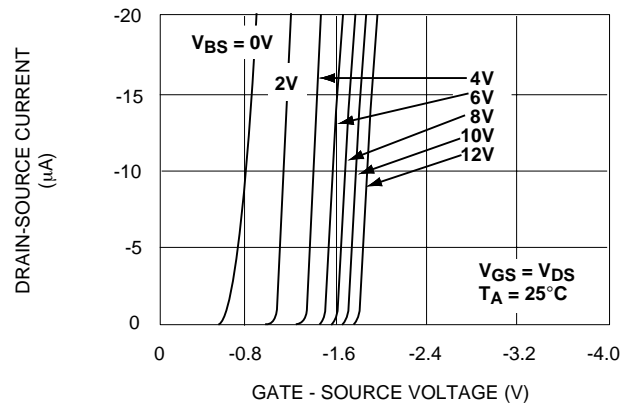
LOW VOLTAGE OUTPUT CHARACTERISTICS



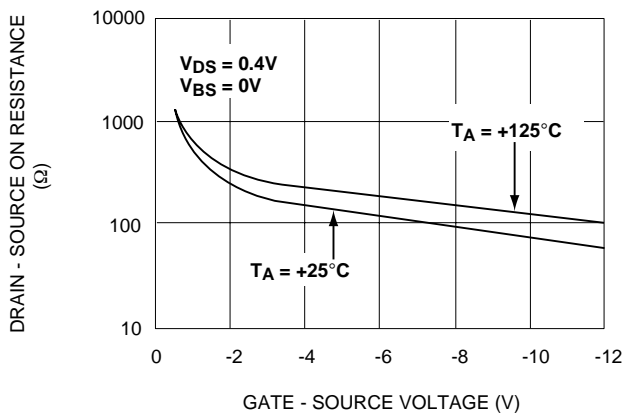
FORWARD TRANSCONDUCTANCE vs. DRAIN - SOURCE VOLTAGE



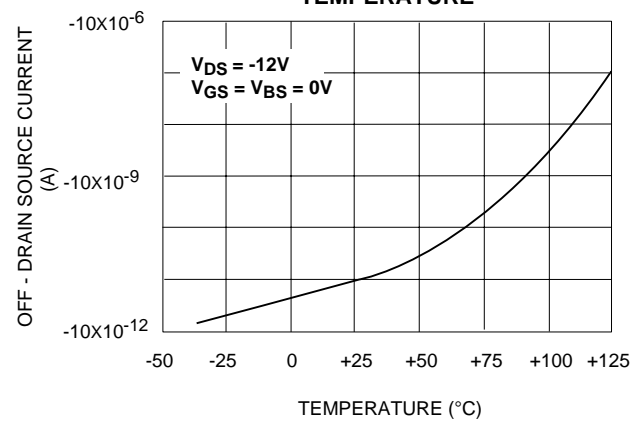
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



RDS (ON) vs. GATE - SOURCE VOLTAGE

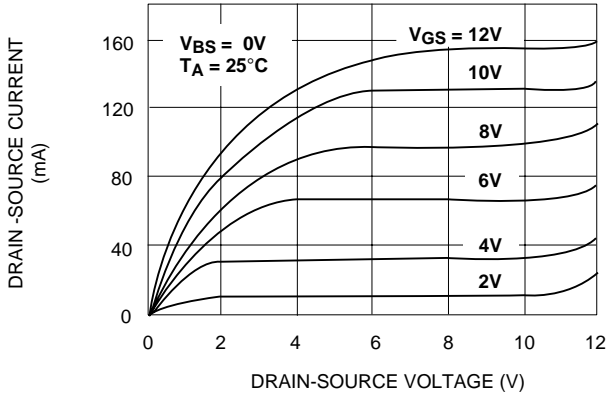


OFF DRAIN - CURRENT vs. TEMPERATURE

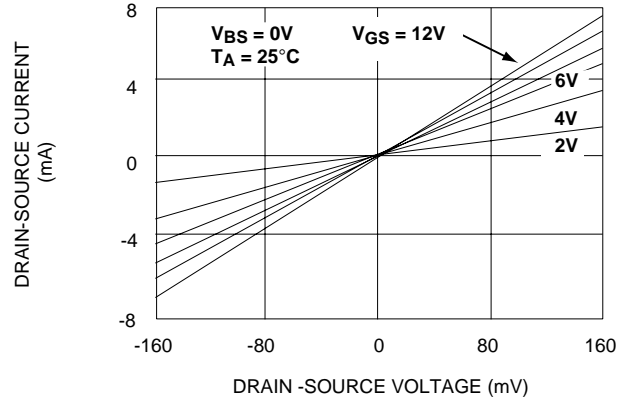


TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS

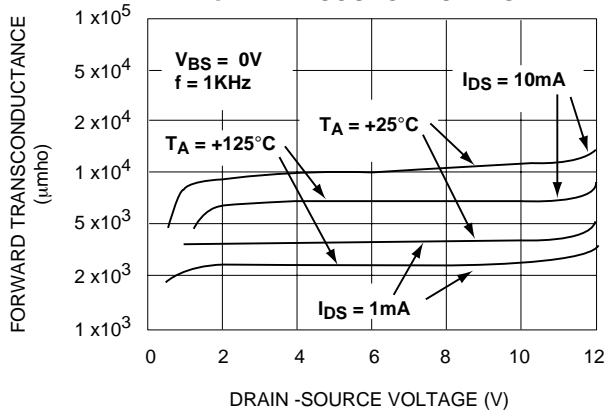
OUTPUT CHARACTERISTICS



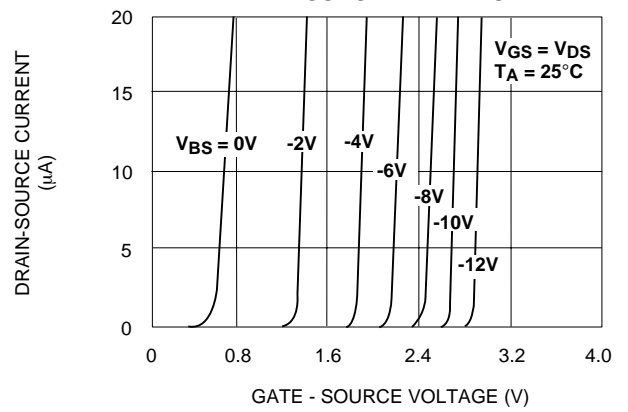
LOW VOLTAGE OUTPUT CHARACTERISTICS



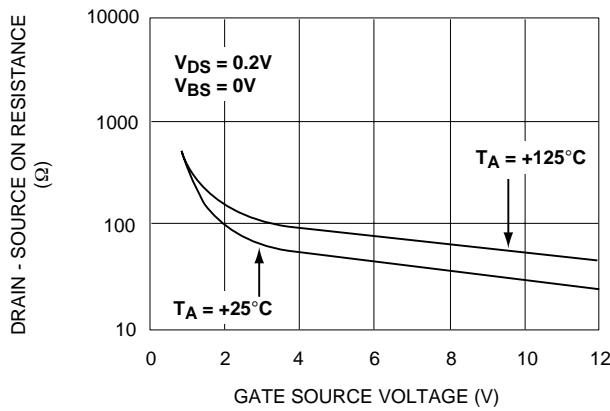
FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE



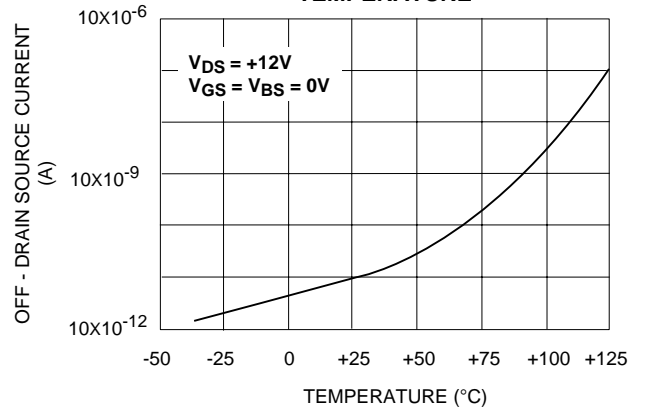
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



RDS (ON) vs. GATE - SOURCE VOLTAGE

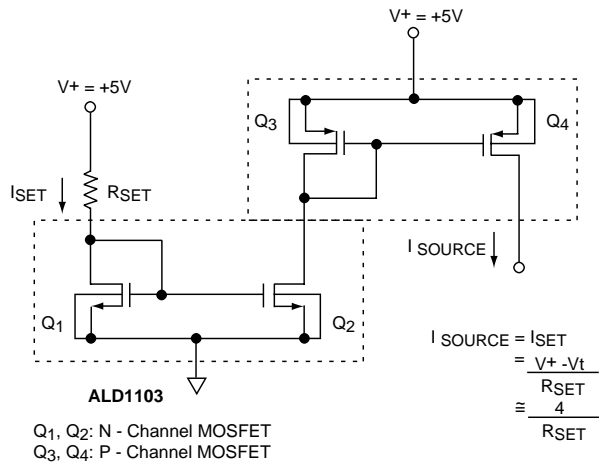


OFF DRAIN - CURRENT vs. TEMPERATURE

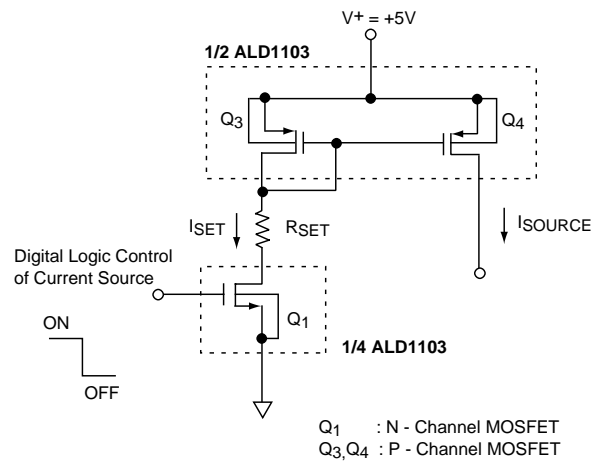


TYPICAL APPLICATIONS

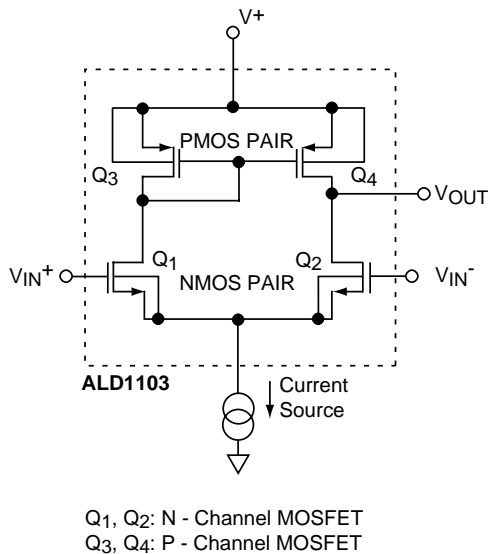
CURRENT SOURCE MIRROR



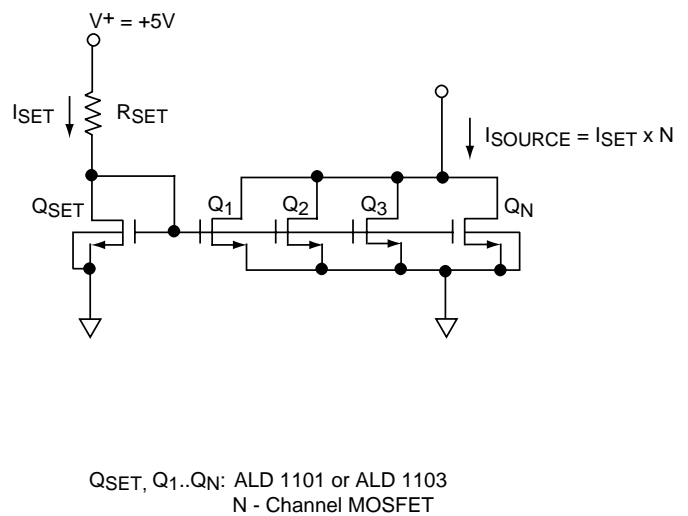
CURRENT SOURCE WITH GATE CONTROL



DIFFERENTIAL AMPLIFIER



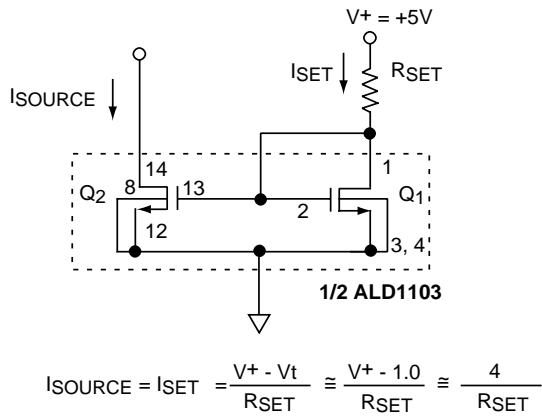
CURRENT SOURCE MULTIPLICATION



TYPICAL APPLICATIONS (cont.)

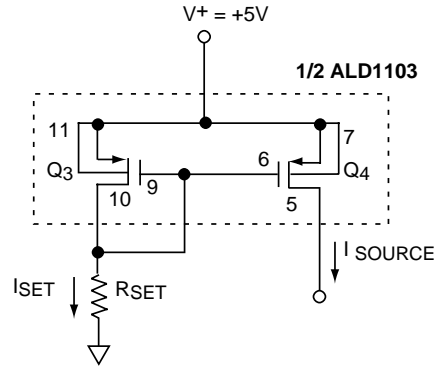
BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE



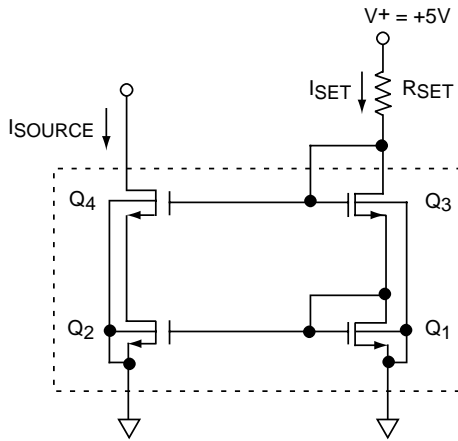
Q1, Q2 : N - Channel MOSFET

P-CHANNEL CURRENT SOURCE

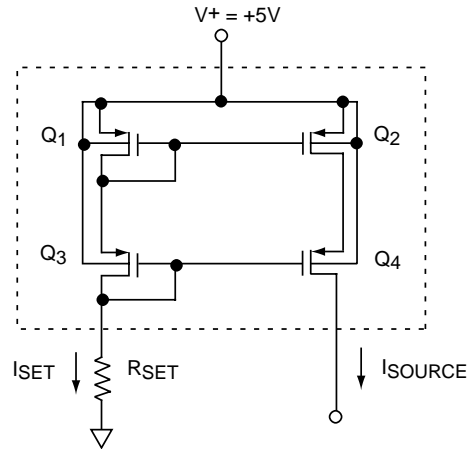


Q3, Q4: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q1, Q2, Q3, Q4: N - Channel MOSFET
(ALD1101 or ALD1103)

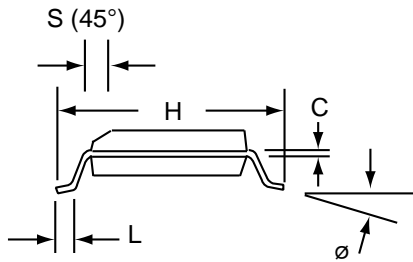
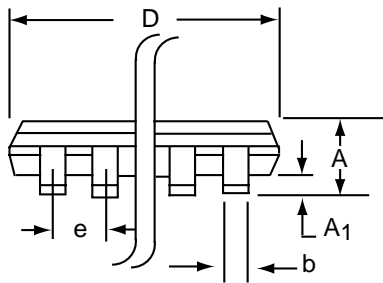
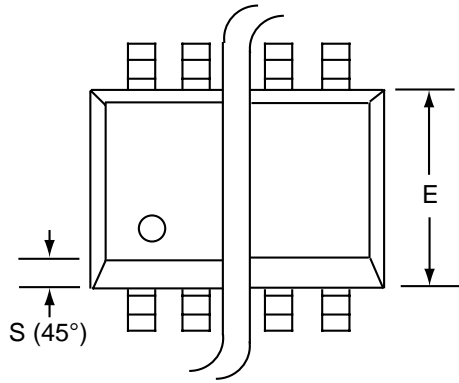


$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2V_t}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET
(ALD1102 or ALD1103)

SOIC-14 PACKAGE DRAWING

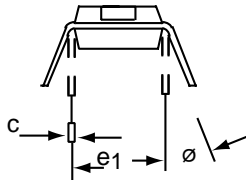
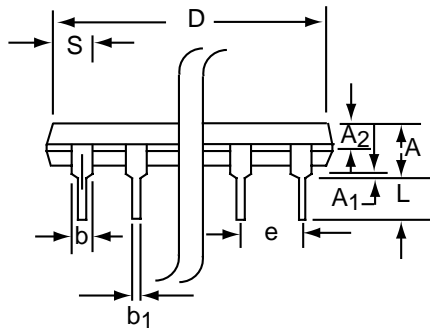
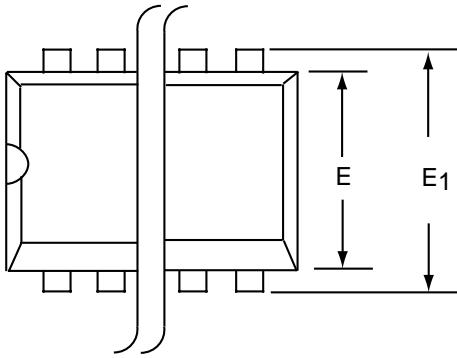
14 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

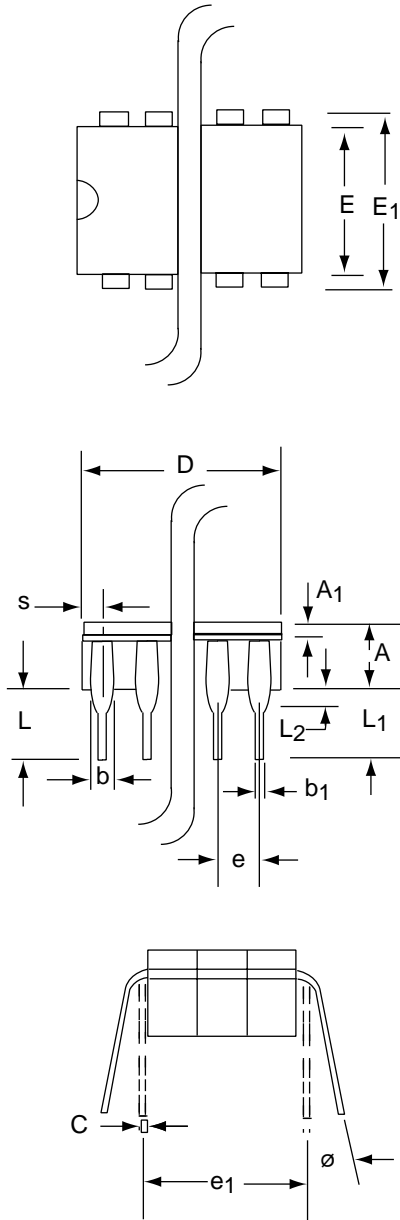
14 Pin Plastic DIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A ₁	0.38	1.27	0.015	0.050
A ₂	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b ₁	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E ₁	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e ₁	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A₁	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b₁	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E₁	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e₁	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L₁	3.18	--	0.125	--
L₂	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
∅	0°	15°	0°	15°