Category: Timer Oscillator **CIRCUIT IDEAS FOR DESIGNERS** Schematic no. time_15001.0

# Time Delay Generator

## Description

This is a basic time delay generator using voltage comparators. This example uses a quad voltage comparator. The first input stage produces an RC time delay. In this example, this time delay is determined by R=50K+$R_T$ and C= $C_T$. When the voltage of this RC network charges past threshold voltages set by resistor network $R_F1$, $R_F2$, $R_F3$, $R_F4$, each of the voltage comparator is triggered on in a sequence, depending on the respective voltage set at the negative input terminals of each voltage comparator by the $R_F$ resistor values. This time delay generator produces outputs V1, V2 and V3 that has a fixed relative time delay to each other as they are triggered by the same input voltage stage. Time delay of V2 always exceeds time delay of V3 because its reference voltage at its negative input terminal is set by the addition of resistor $R_F3$. Likewise, time delay of V1 always exceed that of V2 and V3 because of addition of $R_F2$ to its reference threshold setting.

For full schematic diagram and notes, please register and login at aldinc.com