Category: SABFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. sabfet_11101.0

Balancing 2-Supercap Series Stack

Description

A dual supercapacitor auto balancing (SAB) MOSFET array connects across two-supercaps in series, using the ALD 9100xx series, with xx equal to the threshold voltage, V_t, in 0.10V increments. At V_t, the I_{DS} ON current for SAB MOSFETs M1(top) and M2(bottom) is set at 1µA. The I_{DS} ON current of M1/M2 change exponentially with slight changes in the gate-source voltage, V_{GS}. The equivalent circuit on the right shows M1/M2 behaving like voltage sensitive resistors. At V_{GS} voltages below or above V_t, the SAB MOSFET I_{DS} ON current changes at a rate of approximately 1 decade for every 0.1V change in V_{GS}. When V_{GS} drops low enough, the I_{DS} ON current becomes essentially zero. For example, the ALD910025 has a V_t of 2.50V. If its V_{GS} voltage falls below 1.9V, the I_{DS} ON current decreases to pA range, which is near zero compared to 1µA. ALD910025 can be used to balance supercaps at different voltages such as 2.3V, 2.4V, 2.5V, 2.6V and 2.7V for different nominal leakage current ranges.

If the top supercap C1 has a higher internal $I_{LEAK(top)}$ than the bottom supercap C2, the $V_{S(top)}$ drops below that of $V_{S(bottom)}$, which then reduces the I_{DS} ON of M1. With V+ = +5.0V = 2*V_S = $V_{S(top)}$ + $V_{S(bottom)}$, $V_{S(bottom)}$ must then increase, thereby increasing the I_{DS} ON of M2. This causes the excess $I_{LEAK(top)}$ from C1 to leak through M2. In equilibrium, $V_{S(top)}$ is at a voltage little lower than $V_{S(bottom)}$ where the difference in V_S voltages reflect differences in relative supercap leakage currents. V1, equal to $V_{S(bottom)}$, settles to approximately the mid-point of V+. The ALD910025 or the ALD910026 can both be used for V_S nominal values of 2.5V, with ALD910026 having less leakage range. In equilibrium, the total leakage current across both M1/M2 and C1/C2 network is approximately equal to the highest leakage current of any one of C1/C2.

For full schematic diagram and notes, please register and login at aldinc.com