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Whitepaper
Title: New Plug & Play Solution for Balancing Supercapacitors
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New PCB Provides Plug & Play Solution For Balancing Supercapacitor Cells

Supercapacitors are a great alternative to batteries in applications needing many rapid charge/discharge cycles and are popular in applications such as short-term energy storage, regenerative braking, and static RAM memory backup.

But adding a supercapacitor to a design involves more than connecting a few wires. A supercapacitor has a specified operating voltage of 2.5V – 2.7V, so most applications use an array of devices connected in series for higher voltage.

Each supercapacitor has a leakage current which varies based on numerous factors, including:

- Aging
- Initial leakage value
- Supercapacitor chemistry, material, and construction
- Leakage variation with charging voltage, charging current and temperature
- Operating temperature range

In an array, differences in leakage currents between individual cells result in differences in voltages across them over time; this can cause reduced lifetime and eventual failure since exceeding the maximum voltage on a supercapacitor can lead to cell rupture.

Preventing this imbalance requires a balancing circuit that keeps the voltage across each supercapacitor within limits by automatically correcting for the effects of changing leakage currents, all with minimal added leakage current or power consumption.

For the module designer, this represents an additional layer of complexity. A simple resistor-based design dissipates power and doesn't respond to aging and temperature variations; an opamp-based design has higher performance, but is complicated, also wastes power and consumes excessive board space. Developing a solution also requires layout expertise and analog or power design skills; the result may be added development time or even make the problem worse and add unwanted leakage of its own.

Overview of the SABMB16 Auto-Balancing PCB

A new printed circuit board (PCB) offers a "plug and play solution" by combining all of the circuitry required to accomplish these tasks for any size supercapacitor. Figure 1 shows the SABMB16, which is designed to be used in conjunction with a MOSFET array such as ALD's ALD8100XX or ALD9100XX family.

Each board measures only 0.6" x 1.6" and when fully populated can balance up to four supercapacitors connected in series; in addition to the unpopulated SABMB16, populated boards are available with different combinations of MOSFETS for different operating voltages. For larger arrays, any number of SABMB16 boards can be connected in series, subject only to a maximum voltage per board of 15V.

Figure 1: The SABMB16 includes MOSFET arrays to balance up to four supercapacitors plus external components.

The SABMB16 can accommodate supercapacitors from 0.1F to 3000F and beyond. The average additional power dissipation due to the use of SABMB boards is zero, which makes this method of supercapacitor balancing very energy-efficient. It is especially suited for low-loss energy harvesting and long-life battery-operated applications.
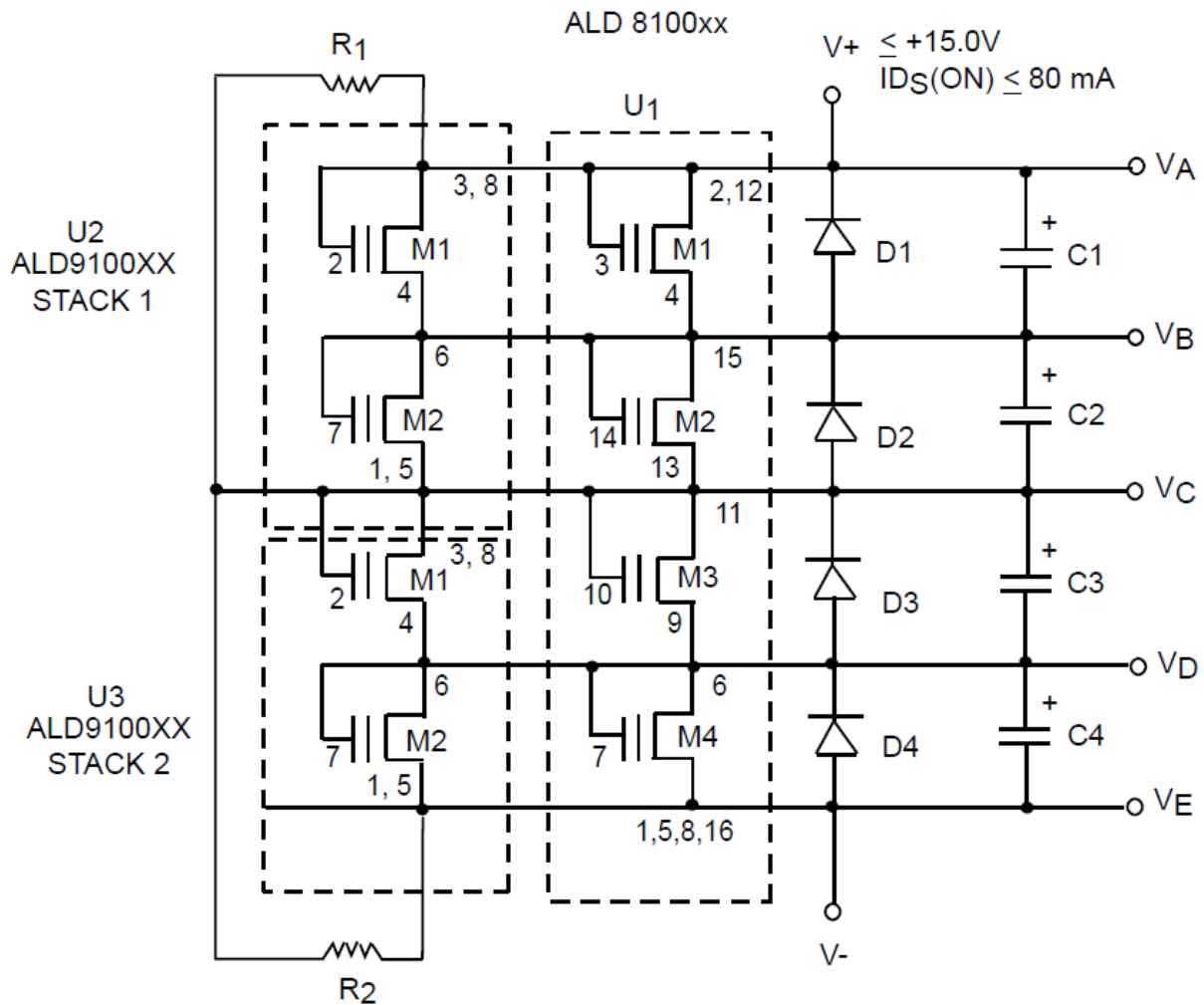

Figure 2: schematic of a fully-populated SABMB16 with three MOSFET arrays. The design ensures that the voltage across each supercapacitor ($V_A - V_B$, for example) does not exceed the maximum allowed value.

Figure 2 shows the schematic of SABMB16 used with four supercapacitors C1 – C4. The ALD8100XX is an array of four identical MOSFETs, each one with its gate and drain connected together; the ALD9100XX contains two devices in an identical configuration.

In an ALD array, each MOSFET is rated for a reverse bias diode current of up to 80 mA maximum. Any reverse bias condition as a result of changing supercapacitor voltages, especially during fast supercapacitor discharge, could lead to some internal nodes becoming reverse biased with surge current in excess of this limit.

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The SABMB16 board has TO277 pads for adding external Schottky rectifiers (power diodes) to clamp such current transients.

An optional resistor can also be connected across each pair of supercapacitors. Normally this is left open, but if those two supercapacitor locations are unpopulated a zero-ohm jumper in the corresponding location should be installed.

Circuit Operation

How does the circuit automatically balance leakage? A MOSFET can be considered as a three-terminal voltage-controlled resistor over a limited operating range, with the "on" resistance $R_{DS(ON)}$ an exponential function of the input voltage V_{GS}. When the gate and drain are connected, V_{DS} is also equal to V_{GS}, and called the threshold voltage V_t. Figure 3 shows the data for the ALD8100XX quad MOSFET array.
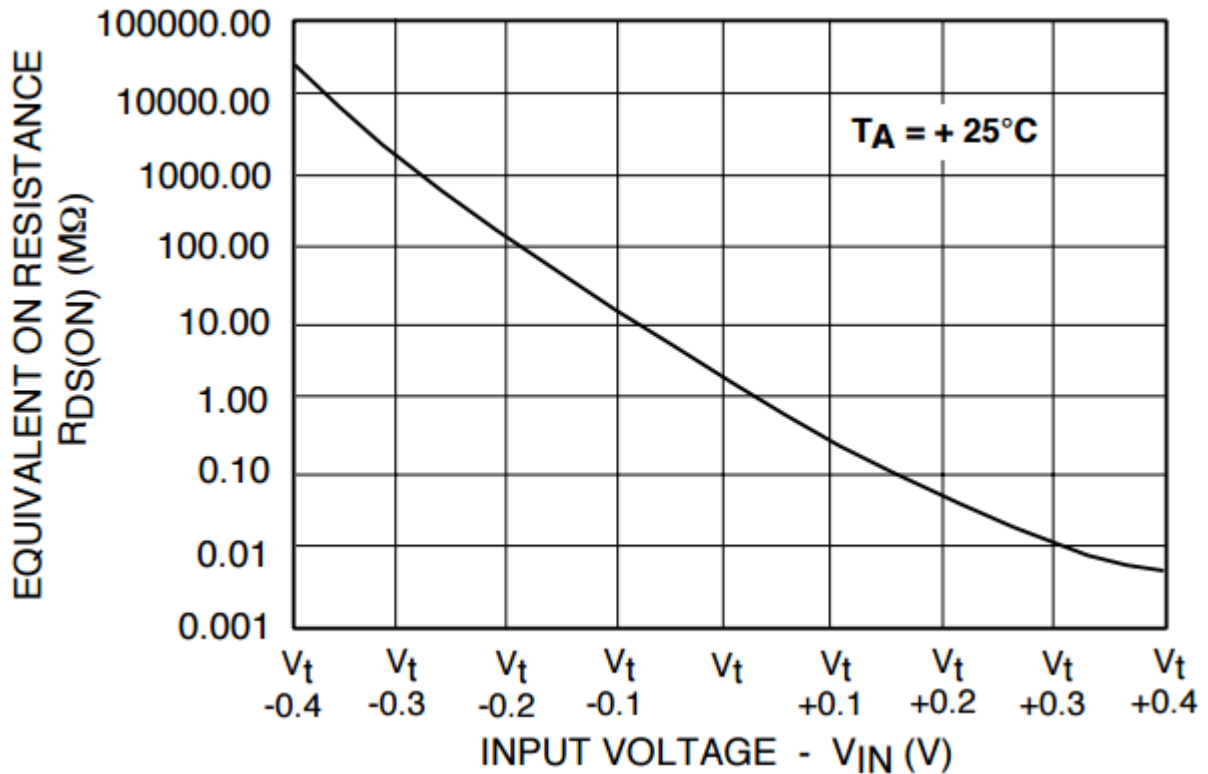

Figure 3: The ALD8100XX relative ON resistance vs. input voltage.

The "XX" in the ALD part numbers denotes the threshold voltage V_t that gives an output current I_{OUT} of 1µA at 25°C. For example, the ALD810025 quad array has $V_t = 2.5V$, so $I_{OUT} = 1µA$ at 2.5V and 25°C. This corresponds to an $R_{DS(ON)}$ of 2.5MΩ. Table 1 shows the change in I_{OUT} as V_t varies.

	Output Current $I_{OUT} = I_{DS(ON)}$ (µA)										
	0.0001	0.001	0.01	0.1	1	10	100	300	1000	3000	10000
V_{IN}(V)	2.10	2.20	2.30	2.40	2.50	2.60	2.74	2.84	3.02	3.32	3.92
$R_{DS(ON)}$ (MΩ)	21000	2200	230	24	2.5	0.26	.027	0.01	0.003	0.001	0.0004

Table 1: Equivalent ON resistance at different input voltages and output currents for the ALD810025 at $T_A = 25°C$.

When a MOSFET is connected across a supercapacitor in an array, the exponential relationship between V_t and $R_{DS(ON)}$ means that any small increase in the supercapacitor voltage caused by leakage current from another supercapacitor will cause a large decrease in the $R_{DS(ON)}$ of that MOSFET. This will increase $I_{DS(ON)}$ and reduce the voltage. As the voltage decreases, $I_{DS(ON)}$ will also decrease.

Depending on the SABMB part number selected, each supercapacitor can have a single MOSFET or two devices in parallel connected across it. Connecting two devices in parallel gives an equivalent MOSFET with twice the output current and twice the sensitivity to voltage change.

The leakage current balancing mechanism is fully automatic and works for supercapacitor arrays with different leakage current profiles. In a stack with many supercapacitors in series, multiple MOSFET arrays function to balance the various leakage currents.

For example, if leakage current I_{C1} is greater than I_{C2} in the four-capacitor array in figure 2, then both M1s (in U1 and U2) are turned off and the M2 pair becomes the active circuit element to balance C1, the supercapacitor with the greatest leakage.

Without the auto-balancing circuit, the voltage across C2 can keep rising until it destroys the part. The MOSFET balancing solution contributes virtually no additional current drain and adjusts for temperature, time, and other environmental changes that may contribute to out-of-balance conditions.

SAB™ MOSFETs

The SAB™ (Supercapacitor Auto-Balancing) MOSFETs in the ALD arrays mentioned above are specifically designed to address the problem of leakage in a supercapacitor array.

The correct SAB™ MOSFET array for a given application depends on supercapacitor rated voltage and leakage; the selection process is discussed in detail in the ALD8100XX/ALD9100XX family data sheet.

By providing a plug-and-play solution to the problem of balancing leakage currents in supercapacitor arrays, the new SABMB PCB with its SAB™ MOSFETs saves both time and effort for designers who must integrate supercapacitors into their module