

Category: Timer Oscillator

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. time_15005.0

Quad Monostable Mode Operation (One Shot Pulse)

Description

This circuit is configured in quad monostable mode of operation, which are four independent basic time delay circuits, each using a 555 type of timer. The single chip quad timer offer excellent timing and temperature tracking between the 4 separate timers. The monostable circuit is also sometimes referred to as a one-shot circuit, as it generates one fixed delay pulse every time it is triggered. In the initial state, the circuit is in the standby mode. The trigger input is at a high level, and the output is at a low voltage level. The discharge output at pin2 (pins 4,6,and 8 for the other 3 timers respectively) is on, and that clamps the capacitor C to ground potential. When a negative going trigger pulse is delivered to input at pin3 (pins5, 7 and 9 respectively), the flip-flop inside the 555 timer is set to turn off the transistor at pin2 and the RC network starts charging towards V+, with a time constant equal to R x C. Capacitor C is charged towards 2/3 V+ and when its voltage reaches that threshold level, the output driver on pin19 (pins 17,15,13 respectively) turns on and the transistor at pin2 is also turned on, discharging C once again to ground potential. The time constant of the pulse width is determined by $t = 1.1 R \times C$, which is the time it takes for the capacitor to charge from 0 to 2/3 V+. This circuit only respond to negative going pulses. Once triggered, the output will remain HIGH until the time delay has elapsed, even if it is triggered again during this time interval. Using CMOS quad 555 timer circuits, a very wide timing range at very low level of voltage spikes and power dissipation can be achieved. Selection of the values of R is limited by the input leakage specifications of the timer at pin2 and pin18, etc. R resistor values are also limited by the internal leakage current at the capacitor C. C usually has a range from $10,000\mu F$ down to 0.

For full schematic diagram and notes, please register and login at aldinc.com

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