

Category: Timer Oscillator

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. time_15002.0

Astable Mode Operation 50% Duty Cycle

Description

This is a basic oscillator circuit using a 555 type of timer. The circuit is configured as an astable multivibrator, with the oscillation frequency given by $f=1/(1.4 \times R \times C)$. Initially, Output at pin3 is at a high-level voltage state, the voltage on C charges towards 2/3 V+. When it reaches that threshold level, the output driver on pin3 is switched to low output voltage state, discharging C. When C is discharged to 1/3 V+, it triggers the comparator inside pin2, which now switches the state of the Output on pin3 again to a high state. This starts the C charging cycle again. Hence through the charging and discharging cycles, an oscillator circuit is implemented. As the charging and discharging cycles involve the same threshold and trigger levels, the oscillator charges and discharges symmetrically, thus producing a 50% duty cycle oscillator. Using CMOS versions of 555 timer circuits, a very wide frequency range at very low level of voltage spikes and power dissipation can be achieved. Selection of the value of R is limited by the input leakage specifications of the timer at pin2 and pin6. R resistor value is also limited by the leakage current at the capacitor C. C usually has a range of values ranging from $10,000\mu F$ down to 0. At C value equal to 0, the timer circuit will oscillate without an external C, and depends on the internal parasitic capacitor inside the 555 timer entirely.

For full schematic diagram and notes, please register and login at aldinc.com

©2005 Advanced Linear Devices, Inc. Information furnished by Advanced Linear Devices, Inc. (ALD) is believed to be accurate and reliable. However, ALD assumes no responsibility for the use of such information nor for any infringement of patent or rights of third parties that may result from its use. No license is granted implication or otherwise under any patent rights of ALD.