Category: SABFET **CIRCUIT IDEAS FOR DESIGNERS** Schematic no. sabfet_11107.0

# Balancing Two 3-Supercap (6 Cell) Stacks in Series

## Description

Three MOSFETs each from two quad supercapacitor auto balancing (SAB) MOSFET arrays connect across two stacks of three-supercaps in series, using two separate packages of ALD 8100xx series, with xx equal to the threshold voltage, $V_t$, in 0.10V increments. At $V_t$, the $I_{DS}$ ON current for each SAB MOSFET M1/M2/M3 for each stack is set at 1µA. The $I_{DS}$ ON current of each of M1/M2/M3 change exponentially with slight changes in the gate-source voltage, $V_{GS}$. Each SAB MOSFET $M_X$ behaves like a voltage sensitive resistor (See sabfet_11101.0). At $V_{GS}$ voltages below or above $V_t$, the SAB MOSFET $I_{DS}$ ON current changes at a rate of approximately 1 decade for every 0.1V change in $V_{GS}$. When $V_{GS}$ drops low enough, the $I_{DS}$ ON current becomes essentially zero. For example, the ALD810027 has a $V_t$ of 2.70V. If $V_{GS}$ falls below 2.1V, the $I_{DS}$ current decreases to pA range, which is near zero compared to 1µA.

The voltages across M1/M2/M3 for each stack automatically self-adjust to accommodate different leakage currents for each supercap C1A/C2A/C1B/C2B/C3A/C3B. $V_A$ settles to approximately ½ (V+), depending upon relative leakage currents of each supercap in both stacks. The currents through M1/M2/M3 for each stack automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding $V_{GS}$ voltage of $M_X$ connected across it, at a higher $I_{DS}$ ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower $I_{DS}$ ON currents in the corresponding SAB MOSFET until $I_{DS}$ ON ≈ 0. In equilibrium, the total leakage current across both M1/M2/M3 and C1/C2/C3 of each network is approximately equal to the highest leakage current of any one of C1A/C2A/C3A/C1B/C2B/C3B. Note that the absolute maximum voltage ratings must be observed for each individual SAB MOSFET package at all times.

For full schematic diagram and notes, please register and login at aldinc.com