ADVANCED LINEAR DEVICES, INC.

Design Innovations in Analog Semiconductors

ALD810028 Balances Three 2.7V Supercaps in Series

Description

Three supercaps connected in series are balanced using three MOSFETs of the quad supercapacitor auto balancing (SAB) MOSFET ALD810028. The ALD810028 has a threshold voltage, V_t, equal to 2.80 volts. When the gate-source voltage, V_{GS}, is equal to V_t, the I_{DS} ON current for each SAB MOSFET M1/M2/M3 is set at 1µA. The I_{DS} ON current of M1/M2/M3 change exponentially with slight changes in V_{GS}. Each SAB MOSFET M_X behaves like a voltage sensitive resistor (See sabfet_11101.0). At V_{GS} voltages below or above V_t, the SAB MOSFET I_{DS} ON current changes at a rate of approximately 1 decade for every 0.1V change in V_{GS}. In this example, the V_{GS} voltage of each SAB MOSFET M1/M2/M3 is set at approximately 2.7V, which has a nominal I_{DS} ON current of 0.1 µA. If the V_{GS} voltage for the ALD810028 falls below 2.2V, the I_{DS} current decreases to pA range, which is near zero compared to 1µA.

The voltages across M1/M2/M3 automatically self-adjust to accommodate different leakage currents for each supercap C1/C2/C3. V_1 and V_2 settle to approximately $^2/_3$ (V+) and $^1/_3$ (V+) respectively, depending upon relative leakage currents of each supercap in the stack. With V+ equal to 8.1V, V_1 is 5.4V and V_2 is 2.7V. The currents through M1/M2/M3 automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding V_{GS} voltage of M_X connected across it, at a higher I_{DS} ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower I_{DS} ON currents in the corresponding SAB MOSFET until I_{DS} ON ≈ 0. In equilibrium, the total leakage current across both M1/M2/M3 and C1/C2/C3 network is approximately equal to the highest leakage current of any one of C1/C2/C3.

For full schematic diagram and notes, please register and login at aldinc.com