



Category: SABFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. sabfet_11105.0

Balancing Two 4-Supercap (8 cell) Stacks in Series

Description

Two quad supercapacitor auto balancing (SAB) MOSFET arrays connect across two stacks of 4-supercaps in series, using two separate packages of ALD 8100xx series, with xx equal to the threshold voltage, V_t, in 0.10V increments. At V_t, the I_{DS} ON current for each SAB MOSFET M1/M2/M3/M4 for each stack is set at 1µA. The I_{DS} ON current of each M1/M2/M3/M4 change exponentially with slight changes in the gate-source voltage, V_{GS}. Each SAB MOSFET M_x behaves like a voltage sensitive resistor (See sabfet_11101.0). At V_{GS} voltages below or above V_t, the SAB MOSFET I_{DS} ON current changes at a rate of approximately 1 decade for every 0.1V change in V_{GS}. When V_{GS} drops low enough, the I_{DS} ON current becomes essentially zero. For example, the ALD810024 has a V_t of 2.40V. If its V_{GS} voltage falls below 1.8V, the I_{DS} current decreases to pA range, which is near zero compared to 1µA.

The voltages across M1/M2/M3/M4 for each stack automatically self-adjust to accommodate different leakage currents for each supercap C1A/C2A/C3A/C4A/C1B/C2B/C3B/C4B. V_A settles to approximately $\frac{1}{2}$ (V+), depending upon relative leakage currents of each supercap in both stacks. The voltages across each SAB MOSFET M1/M2/M3/M4 for each stack automatically control the voltage across each supercap. A higher supercap voltage results in a higher corresponding V_{GS} voltage of M_x connected across it, at a higher I_{DS} ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower I_{DS} ON currents in the corresponding SAB MOSFET until I_{DS} ON \approx 0. In equilibrium, the total leakage current across both M1/M2/M3/M4 and C1/C2/C3/C4 of each network is approximately equal to the highest leakage current of any one of C1A/C2A/C3A/C4A/C1B/C2B/C3B/C4B. Note that the absolute maximum voltage ratings must be observed for each individual SAB MOSFET package at all times.

For full schematic diagram and notes, please register and login at aldinc.com

©2013 Advanced Linear Devices, Inc. Information furnished by Advanced Linear Devices, Inc. (ALD) is believed to be accurate and reliable. However, ALD assumes no responsibility for the use of such information nor for any infringement of patent or rights of third parties that may result from its use. No license is granted implication or otherwise under any patent rights of ALD.