Nano-Power Voltage Comparators, Voltage Detectors and Voltage References using EPAD® MOSFETs

Advanced Linear Devices, Inc.

Introduction

The quest to achieve ever-lower operating voltage and lower power consumption levels in circuit design is a trend that has placed difficult challenges on electrical engineers. This is especially true for battery operated and Energy Harvesting operated applications where detecting and sensing a minute signal at minimal power consumption poses a significant technical challenge. For applications such as surveillance, security alarms and event sensing, where the signal needs to be continuously sensed, but the event occur very infrequently, a better approach to power management in the design and powering of the electronics involved can pay big dividends for the designer and the user.

Many applications also fall into the category of Zero Power Normally-On circuits where there is No power consumed when the circuit is in the On state. This is ideal for many battery operated circuits where the battery charge must be conserved to provide for long service periods.

The paradigm that EPAD MOSFET arrays introduce is that gate thresholds can now be precisely controlled so that analog designers are now able to take advantage of the absolute value of the gate threshold voltage as a design parameter. The actual gate threshold voltage also can be relied on as an on-off control reference voltage.

Novel but extremely simple circuit designs are presented to illustrate how these devices can be used at a practical level as a way of describing what is possible with these revolutionary new EPAD MOSFET arrays.

GENERAL DESCRIPTION

ALD EPAD® MOSFET Arrays are a unique family of monolithic quad/dual N-Channel ZeroThreshold™ mode, ENHANCEMENT mode and DEPLETION mode MOSFET devices. These MOSFETs are precision matched at the factory using ALD's proven EPAD® CMOS technology. This family offers tightly controlled threshold voltages, which enables predictable transistor operation at very low voltages and currents.

Enhancement Mode ALD1108xx Quad/ ALD1109xx Dual

The ALD1108xx/ALD1109xx products are precision enhancement mode MOSFET devices No conductive channel exists between the source and drain at zero applied gate voltage. This precise threshold voltage feature enables designs that have reduced circuit complexity. Often supply voltages and supply currents can also be greatly reduced.

Depletion Mode ALD1148xx Quad/ ALD1149xx Dual

ALD1148xx/ALD1149xx products are precision depletion mode MOSFETs, which are normally-on devices when the gate bias voltage is at 0.0V, which exhibit a controlled on-resistance between the source and drain terminals. The depletion mode threshold voltage is at a negative voltage at which the MOSFET device turns off.

Key Performance Characteristics

The EPAD® MOSFET Arrays are designed for tight matching of device electrical characteristics, built for minimum offset voltage, low differential thermal response and excellent temperature coefficient tracking characteristics.

I – V Characteristics

The graphs in **Figures 1 – 3** show the electrical characteristics of the EPAD® MOSFET Array family. In Figure 1, the graph depicts an ALD1108xx MOSFET turn-on drain current versus drain voltage characteristics as a function of gate voltage at or above threshold voltage. With threshold voltage precisely controlled, the drain current control at a given gate voltage input is precise as well.

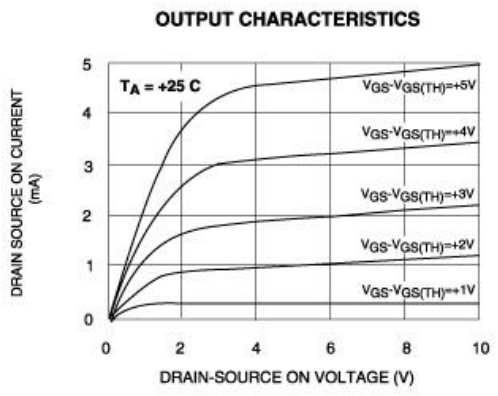

FIGURE 1

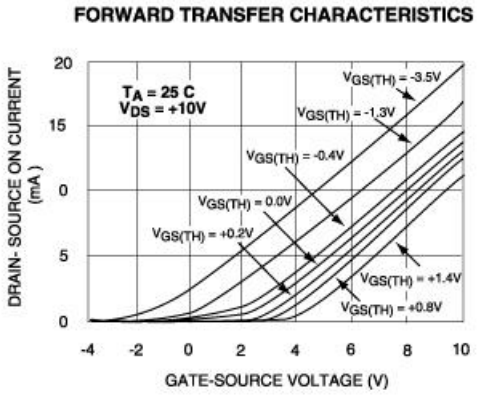

FIGURE 2

The drain current of an EPAD MOSFET in the linear region (where Vds < Vgs – Vgs(th)) is given by:

$$Ids = (k.W/L).[Vgs - Vgs(th) - Vds/2].Vds$$

where
k = u. Cox
u is the carrier mobility
Cox is capacitance per unit area of gate electrode
Vgs is the gate to source voltage
Vth is the turn-on threshold voltage
Vds is the drain to source voltage
W and L are the channel width and the channel length respectively

This region of the device characteristics, where Ids increases with increasing Vds, is called the linear region, or the triode region. For small values of Vds, the relationship of Vds to Ids is approximated to that of a linear resistor, In other words, the Ids value is proportional to Vds value and the device can be used as gate-voltage controlled resistor.

For higher values of Vds where Vds >= Vgs – Vgs(th), the channel will be nearly pinched off at the drain side, and the output current level will saturate, or pinch off. In this pinched-off region of device characteristics (or saturation region), the Ids current will not increase much as a function of further increases of Vds.

The saturation current Ids is given by approximately:

$Ids = (k.W/L).\ [Vgs - Vgs(th)]^2$

Sub-threshold Voltage Operation

Figure 3A and 3B show that at or below threshold voltage, the MOSFET exhibits a turn-off characteristic called the sub-threshold region. The MOSFET conduction channel rapidly decreases exponentially as a function of the applied gate voltage at a fixed rate of approximately 110 mV per decade of current decrease.

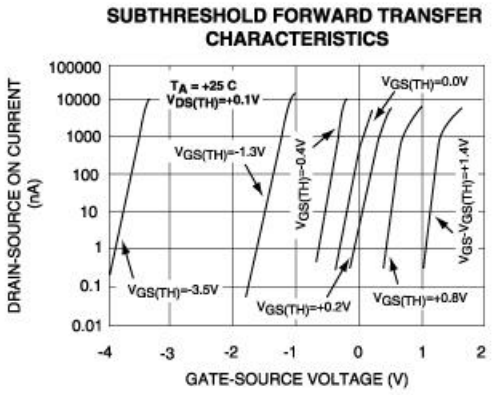

FIGURE 3A

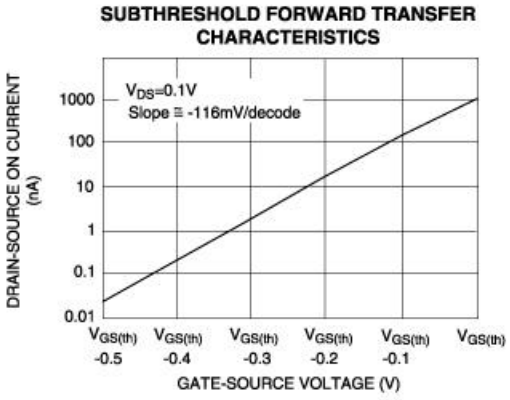

FIGURE 3B

Figure 3A shows the sub-threshold voltage characteristic of all members of the EPAD® MOSFET Array family. **Figure 3B** show an expanded view of the graph in **Figure 3A** for the ALD110802, as an example, with Vgs(th) = +0.2V.

At a drain current selected as "zero current" by the circuit designer, the Vgs voltage at zero current can now be determined. For example, if the zero current of a specific design is 10 nA, then the Vgs voltage at that current level is approximately 220 mV below Vgs(th). Note that in this example where the Vgs(th) = 0.2V, its Ids still hovers around 20 nA when the gate voltage is at zero volt (ground).

With precision control of Vgs(th), it is now easier to bias and operate a MOSFET in the sub-threshold region. Some of the key features and considerations in operating in the sub-threshold region are:

* Very low operating supply voltages
* Very low signal voltage swings
* Very low operating current levels involved
* Ultra low power consumption
* Very high impedances at inputs and outputs without using high-valued resistors

* Exponential I to V characteristics
* Unique transconductance.

Ultra Low Supply Voltage

Operating Ultra Low Supply Voltage systems implies a MOSFET threshold voltage that must correspond to its voltage transition needs. Hence a +0.2V Supply System must have threshold voltages that would operate at +0.2 V.

Several EPAD® MOSFETs are designed for very low supply voltage situation. The ALD110802, for example, has a turn-on threshold voltage of only +0.2V, which, depending on the circuit biasing conditions, can accept or produce greater than 0.8V signal swing with a 1 V supply. Using the ALD110800 ZeroThreshold™ MOSFET, a rail-to-rail 1V signal swing can be achieved in many circuit configurations with only a 1V supply.

As an example, a single panel solar cell that put out about 0.45V when loaded can be used to build useful circuits with an EPAD® MOSFET. The +0.45V can be used in a single supply configuration, or split into +/- 0.225V dual supplies. Another example would be an inverter circuit using an ALD110800 device to operate with a mere 50 mV power supply.

Low Power and NanoPower™

When supply voltage decreases, the power consumption of a given load resistance decreases as the square of the supply voltage. So one of the key benefits in reducing supply voltage is to reduce power consumption. Although usually decreasing power supply voltages and power consumption go hand-in-hand with decreasing useful AC bandwidth and increasing noise in the circuit, a designer can make the necessary tradeoffs for a given circuit application and bias the circuit accordingly to optimize a number of variables.

From the previous paragraphs a scenario emerges where low supply voltages, in conjunction with the appropriate MOSFET devices, along with careful circuit design to bias different branches of the circuit optimally, a circuit that performs a certain function can be designed so that power consumption can be minimized.

A circuit can be designed using different members of the ALD EPAD® MOSFET Array family so that power consumption is minimized. Circuits operating in nano-watt mode can be built and still provide a well-biased and controlled circuit function.

MOSFET Inverter as a Nano-power Voltage Comparator

A basic MOSFET inverter consists of either a resistor or a MOSFET load and a MOSFET as the inverting device. By selecting a device with a precision Vgs(th), it may be possible to create an inverter running at ultra low voltage levels, ultra low power levels, or both. There are infinite numbers of possible combinations of voltage and power levels with various Vgs(th), with the choice determined by the mission of the circuit.

Figure 5A is an example to illustrate some of the possibilities. In one example, the basic inverter work as a digital logic inverter and is powered with a V+ of only 200 mV, with I+(max) = 0.24 uA, resulting in an average power of about 25 nW(nanoWatt), assuming a 50% duty cycle signal. Another example of this basic inverter specifies the Vgs(th) to be at +0.4V and working with a load resistor of 44MEG Ohm, results in an average current of 2.3 nA and total power of 0.45 nW, using the same 200 mV supply.

Using the same inverter with a photodiode at its input and a 1.5V battery, this inverter now become an inverting amplifier acting as a voltage comparator, with a built-in voltage reference. This circuit actually functions as a nanopower voltage detector circuit, with the photodiode sensing light input and generating a voltage that the inverter input can sense, amplify and detect. This circuit is particularly suitable for alarm and fault detection type of applications, as in the normal operating mode, the circuit practically burns zero power, saving battery power.

The following is a brief description of the functioning of this voltage comparator circuit. The photodiode connects directly to the Gate input of the MOSFET inverter. The photodiode is biased in the voltage mode, with near zero output voltage (~10mV) when there is little or no light input. When a pre-determined level of light input is sensed by the photodiode, a voltage develops across the photodiode. As the Gate input of the MOSFET has very high input impedance, requiring only pA of input bias current, the photodiode operates essentially in the open circuit mode. As photons reach the photodiode, a voltage develops across the photodiode. At a pre-determined, or calibrated light level, the voltage across the diode reaches a sub-threshold voltage level where the drain-source current of the MOSFET reaches an exponential region. In this region, the drain-source current changes by one order of magnitude for each 110 mV change in Gate voltage. An appropriately selected load resistor with a value operating within this region would develop a relatively large voltage swing for a small change in Input voltage. This voltage level can be set by the designer, provided that the sub-threshold voltage slope can be captured. This circuit works only when a precision MOSFET threshold voltage can be produced such that the parametric errors of the circuit elements would not render the circuit in-operative.

A brief description of a photodiode would illustrate the functioning of the light sensing source. When no light reach the photodiode, there is no voltage or a very small voltage developed across the photodiode, typically between 100mV to 150mV. Total darkness would correspond to zero voltage output of 0.0V to a few mV. When the light level reaches, for example, a 500 lux level (indoor fluorescent light) a voltage of about 300 mV is produce. Bright sunlight would produce perhaps 440 mV.

For such a sensor, a detection voltage level of 190 mV may be used to detect the presence or the absence of indoor fluorescent light. When the light level sensed is below the detection level of 190 mV, the MOSFET Gate input voltage is at 190 mV, which is in the sub-threshold region of the MOSFET, with a drain-source bias current at about 20 nA. A 10 Meg Ohm load resistor would produce a voltage drop of 200 mV. Therefore the total maximum current consumption of this comparator circuit is 30 pA for gate input current, plus 20 nA for the drain bias current, when the photodiode is in the “light detecting mode”. A battery powering this circuit would burn about 20 nA x 1.5V = 30 nW as maximum power!

When light input to the photodiode reaches a detection level, the Gate input to the MOSFET is now biased at 290 mV, which generates a drain-source current of

about 130 nA. The voltage drop generated across the load resistor is now 1.3V, and hence the output voltage is now at about 0.3V. This voltage comparator produces an output level of 1.3V for a "0" and 0.3V for a "1".

Using the basic inverter as a buffer provides high level of isolation between the input and output. The input bias current to the inverter is specified at 5 pA typical and 30 pA maximum. The input voltage can be biased at a level convenient for the input source. For example, if the input source is a 50 mV peak to peak signal, centered at ground potential, then using ALD110800 zero threshold MOSFET may help eliminate an input level shift stage and the associated noise and distortion that such a intermediate stage can add to the input signal. In a second example, where the input is a modulating signal, a depletion mode MOSFET is used to help bias the output to a desired voltage level and output impedance.

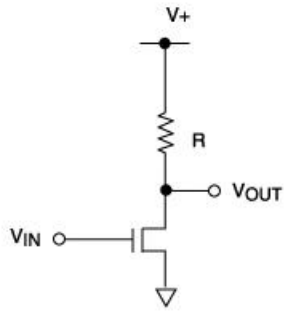

FIGURE 5A

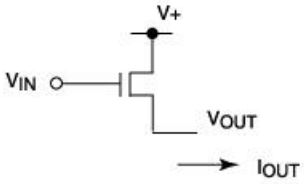

FIGURE 5B

The output level in a basic buffer can be designed to produce the proper output voltage range in part by using an appropriate load resistor and by selecting a specific member of the EPAD® MOSFET Array family. The output voltage can be biased and shifted to any voltage output level and output swing range by design.

The basic inverter can also function as a crude inverting amplifier by biasing the MOSFET transistor in the linear region. This inverting amplifier function is easier to implement using low threshold devices such as the ALD110802 (Vgs(th) = 0.2V) or the ALD110800 (Vgs(th) = 0.0V). As an example of a suggested biasing scheme, the output load resistor can be selected so that the output voltage is nominally at V+/2 when Vin = 0.0V. The inverting amplifier can produce 5x to 12x gain.

A simple voltage source with a MOSFET can be implemented with a MOSFET connected as a source follower where the output currents are supplied by drain to source currents (**Figure 5B**). This circuit is analogous to the classic emitter follower using a bipolar transistor. In this case the input (source) voltage and its source impedance are completely isolated from the output voltage and output currents due to the extremely high input impedance of the MOSFET. The impedance transformed Vout and Iout are dependent only on the input voltage and the output impedance of the MOSFET.

Nano-Power Two-Input Digital Logic Comparator

By extension to the basic inverter, a simple logic gate such as a NAND and a NOR gate can be readily implemented. While digital logic circuit implementation is not the primary application focus for the EPAD® MOSFET Array family, there may be situations where an unconventional logic function that operates on 0.4V or less power supply is useful.

In **Figure 6 and 7** the EPAD® MOSFET Array family devices are configured to implement logic functions. A single MOSFET array can be used to implement both NOR and NAND gates connected in a compound configuration. **Figure 6** illustrates a two-input NOR gate and **Figure 7** illustrates a two-input NAND gate.

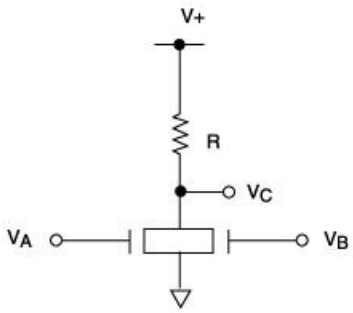

FIGURE 6

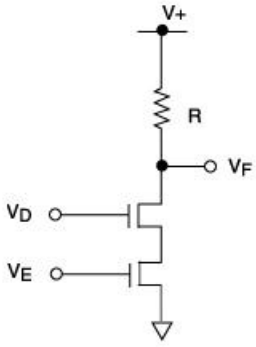

FIGURE 7

A key consideration is to determine the V+ supply available which will power up the logic circuit. When the V+ supply voltage drops to below 400 mV, the MOSFETs are actually likely to be always in the same "off-state". They are biased in the sub-threshold region, whether in the "1" state or the "0" state of logic.

For example, consider the case of a 200mV supply and a MOSFET with threshold of 0.20V (ALD110802). In the output "1" state, the output is near 0.2V and the MOSFET is operating in the low end of the sub-threshold region, with drain current of about 19 nA. In the output "0" state, the MOSFET is operating in the high end of the sub-threshold region, with a drain voltage near 0.0V and a drain current of about 230 nA. When multiple MOSFETs are connected to build logic gates, both the "0" state current and voltage levels and the "1" state current levels must satisfy the desired output voltage and operating temperature range criteria.

The actual drain current in any circuit configuration depends on the actual circuit topography. The operating frequency of such a logic gate implemented depends on the operating voltage and the amount of current switching between the "1" logic state and the "0" logic state.

As the supply voltage decreases below 0.2V, the available voltage and current margins for the logic switching decreases accordingly, and the environment where such a logic gate can be used become more limited and critical. At 0.1V supply, for example, the voltage noise margin between "1" and "0" state drops down to about 50 mV after the first inverter stage. After several more inverter stages, however, this voltage noise margin gradually drops to about 20 mV.

Factors to consider in designing logic function are:

* Threshold voltage and device output tolerances
* Power supply voltage tolerances
* Output voltage level ranges defined to be acceptable for "1" and "0" levels
* Operating temperature ranges
* Number of logic stages and the noise margins required

Basic Normally-On Switch

A normally-on switch is a switch that is normally already turned-on when the gate is at ground voltage or when there is no supply voltage present. This function is analogous to a normally closed FORM B (NC) relay with which the contacts are already closed when the relay coil is not energized, and which requires a voltage source to energize the relay coils in order to open the contacts. Depletion mode MOSFETs are naturally normally-on devices where a conduction channel already exists when there is 0.0V bias on the gate. The resulting conducting channel behaves similarly to a resistor when Vds is at low levels.

However, beware that due to the high input impedance of the gate, the gate voltage can "float" to a value other than zero. In an actual circuit it would be desirable to ground the gate, connect a fixed resistor to the gate or otherwise control the voltage available to the gate.

The key differences between Form B relays and the EPAD® MOSFET Array family are that the MOSFETs have higher on-resistances and operate at low voltages (<10V) and low power levels. In situations where these MOSFETs are used as a substitute for the equivalent function of a normally-on switch, they offer significant benefits such as size, density, power consumption, mechanical ruggedness (all solid-state) and cost. Furthermore, the switch channel on-resistance can be modulated and controlled directly without using other active circuit elements.

Consider the case of building a normally-on switch using a ZeroThreshold™ MOSFET such as the ALD110900. The device is in the on state and conducting a current at about 1uA when the gate is grounded. This is a reliable and dependable current value, and an external sensing circuit can be designed to detect and utilize this current signal.

In the case of using a ZeroThreshold™ MOSFET as a switch, a signal can pass from V+ rail to 0.0V rail with an appropriate circuit configuration. However, a normally-on switch cannot be turned-off unless a negative voltage relative to the source voltage is available to be applied to the gate in order to turn off the MOSFET.

Re-arranging the circuit configuration, a zero threshold MOSFET can also be used as a high-side switch, which can pass a high level signal that is near or at V+ potential. To turn on such a switch, connect the gate to V+ (Vg = V+). Assuming V+ is at least +0.4V, grounding the gate will turn this switch off.

Likewise, other depletion mode MOSFETs can also be used either as high-side switches or as normally-on switches, each having a corresponding normally-on on-resistance value and a corresponding turn-off voltage. Tradeoffs can be made

between on-resistances desired versus the gate voltages required to modulate and/or to turn on and turn off the switch.

Conclusion

This article provides the reader with an understanding and some basic concepts on how useful circuits can be implemented using this EPAD® MOSFET Array family. Many circuits that one has used in the past can also be naturally extended and readily applied here. Due to the extension of voltage and current ranges to lower limits and the precision threshold voltages, a new mindset and a fresh look at many old circuits and their related design configuration issues may be appropriate.

The ultra low voltage and NanoPower™ characteristics of the EPAD® MOSFET Array family and how they can be biased and used in a circuit design can enable new products that feature novel power sources. Many circuits that one has designed in the past can now be naturally extended to new ranges and uses with the ALD EPAD® MOSFET Array family. These family of products begins to offer possibilities in circuit topographies that are quite novel, and in some cases even revolutionary.